IPX CAMERA SERIES

HIGH-RESOLUTION, PROGRAMMABLE 8/10/12 BIT, CAMERA LINK DIGITAL CAMERAS

User's Manual

CONFIDENTIAL NOTICE:

Revision History

RB01	05/03/05	P. Dinev	First Release

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Introduction

This chapter outlines the key features of the IPX camera.

1.1 IPX FAMILY

The IPX series of cameras are built around a robust imaging platform utilizing the latest digital technology. The camera's image processing engine is based on a 1 million gate FPGA.

The IPX family consists of the following 14 cameras:

High Speed:

IPX-VGA120	640x480	120fps	monochrome
IPX-VGA120C	640x480	120fps	color
IPX-VGA210	640x480	210fps	monochrome
IPX-VGA210C	640x480	210fps	color

Mega-pixel:

IPX-1M48	1004x1004	48fps	monochrome
IPX-1M48C	1004x1004	48fps	color
IPX-2M30	1600x1200	30fps	monochrome
IPX-2M30C	1600x1200	30fps	color
IPX-2M30H	1920x1080	30fps	monochrome
IPX-2M30HC	1920x1080	30fps	color
IPX-4M15	2048x2048	15fps	monochrome
IPX-4M15C	2048x2048	15fps	color
IPX-11M5	4000x2672	5fps	monochrome
IPX-11M5C	4000x2672	5fps	color

1.2 GENERAL DESCRIPTION

The IPX cameras are advanced, high-resolution, progressive scan, fully programmable and field upgradeable CCD cameras. They are built around KODAK's line of interline transfer CCD imagers. The camera's image processing engine is based on a 1 million gate FPGA. The IPX cameras feature programmable image resolution, gain, offset, asynchronous external triggering with programmable exposure, and capture duration, electronic shutter, long time integration, strobe output, and gamma correction. A square imager format with uniform 7.4 µm square pixels provides for a superior image in any orientation. The interline transfer CCD permits full vertical and horizontal resolution of high-speed shutter images. The combination of electronic shutter and long time integration enables the cameras capturing speed to be from 1/200,000 second to more than 10 seconds. The cameras have an optically isolated I/O interface (trigger input and strobe output). A built-in Gamma correction optimizes the CCD 's dynamic range. The cameras have a standard Camera Link™ interface that includes 8/10/12 bits data transmission with one or two output taps as well as camera control and asynchronous RS232 serial communication interface, all on a single cable. The cameras are fully programmable via the Camera Link serial interface using a GUI based configuration utility. The adaptability and flexibility of the camera allows it to be used in a wide and diverse range of applications including machine vision, metrology high-definition imaging and surveillance, medical and scientific imaging, intelligent transportation systems, character recognition, document processing and many more.

MAIN IPX FEATURES

- Interline transfer CCD
- Progressive scan image
- 8/10/12 bit data,
- Base Camera Link
- Single or Dual tap operation
- Serial communication
- Horizontal and vertical binning
- Dynamic gamma correction
  - Gamma = 1.0
  - Gamma = 0.45
- Highly programmable:
  - Resolution
  - Electronic shutter
  - Long integration
  - Strobe output
  - Analog gain and offset
  - Area of interest
  - External trigger
    - Pre-exposure
    - Capture duration

CAUTION NOTE

1. IPX cameras sold prior to May 1, 2005 support only 8/10-bit operation.
2. 12-bit was supported by MDC series. This series will be discontinued after May 1, 2005.
3. The new IPX series support 8/10/12-bit.

1.3 IPX TECHNICAL SPECIFICATIONS

A CCD camera is an electronic device for converting light into an electrical signal. The camera contains a light sensitive element CCD (Charge Coupled Device) where an electronic representation of the image is formed. The CCD consists of a two dimensional array of sensitive elements – silicon photodiodes, also known as pixels. The photons falling on the CCD surface create photoelectrons within the pixels, where the number of photoelectrons is linearly proportional to the light level. Although the number of electrons collected in each pixel is linearly proportional to the light level and exposure time, the amount of electrons varies with the wavelength of the incident light. When the desired exposure is reached, the charges from each pixel are shifted onto a vertical register, VCCD, and then one row downwards in a vertical direction towards a horizontal register, HCCD. After that the electrons contained in the HCCD are shifted in a horizontal direction, one pixel at a time, onto a floating diffusion output node where the transformation from charge to voltage takes place. The resultant voltage signal is buffered by a video amplifier and sent to the corresponding video output. There are two floating diffusions and two video amplifiers at each end of the HCCD, and the charges can be transferred towards any of the outputs (depending on the mode of operation). The time interval required for all the pixels, from the entire imager, to be clocked out of the HCCD is called a frame. To generate a color image a set of color filters (Red, Green, Blue) arranged in a "Bayer" pattern, are placed over the pixels. The starting color is Green. Figure 1.1 shows the CCD pixel structure. Table 1.1 shows the individual pixel structure for different IPX cameras. Figures 1.2, 1.3 and 1.4 show the camera's spectral response.

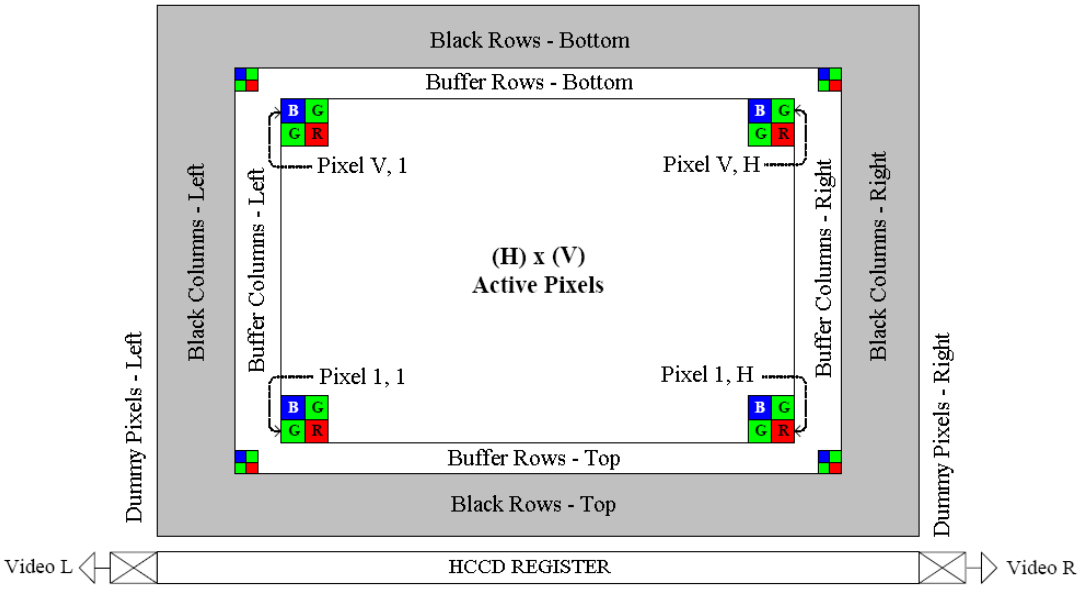


Figure 1.0 - CCD Pixel Structure

Features	IPX-VGA120/VGA210	IPX-1M48	IPX-2M30	IPX-2M30H	IPX-4M15	IPX-11M5
CCD sensor	KAI-0340S/D	KAI-1020	KAI-2020	KAI-2093	KAI-4021	KAI-11000
Pixel size	7.4 µm	7.4 µm	7.4 µm	7.4 µm	7.4 µm	9.0 µm
Black rows - top	4	4	2	4	10	16
Buffer rows - top	4	0	4	2	6	8
Active rows - (V)	**480**	**1004**	**1200**	**1080**	**2048**	**2672**
Buffer rows - bottom	4	0	4	2	8	8
Black rows - bottom	0	0	4	4	0	16
Dummy pixels - left	12	8	4	4	12	4
Black columns - left	24	12	16	28	28	20
Buffer columns - left	4	0	4	4	4	16
Active pixels - (H)	**640**	**1004**	**1600**	**1920**	**2048**	**4000**
Buffer columns - right	4	0	4	4	4	16
Black columns - right	24	12	16	28	28	20
Dummy pixels - right	12	8	4	4	12	4
Frame rate - single	120 fps	30 fps	17 fps	17 fps	7.5 fps	2.5 fps
Frame rate - dual	210 fps	48 fps	33 fps	33 fps	15 fps	5 fps

Table 1.0 - Pixel structure for different IPX cameras.

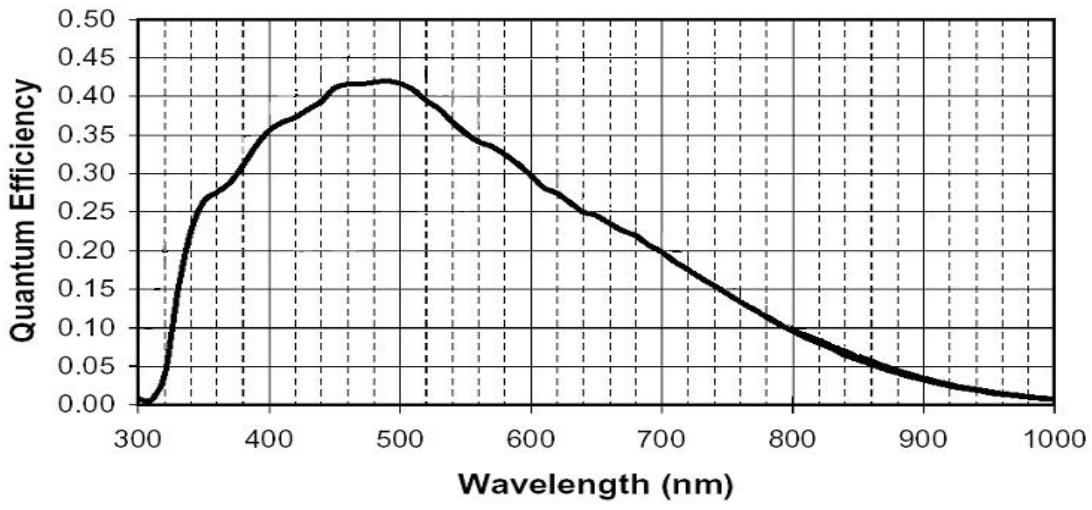


Figure 1.1 - Spectral response – monochrome quantum efficiency
(Measured with the cover glass)

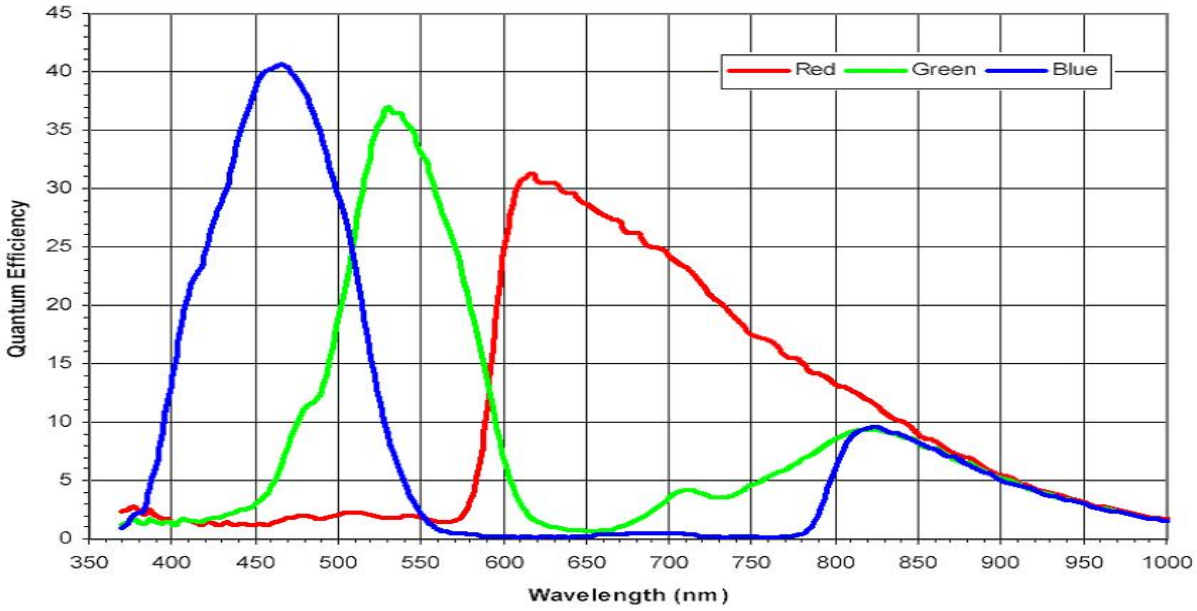


Figure 1.2 - Spectral response – color quantum efficiency
(Measured with the cover glass)

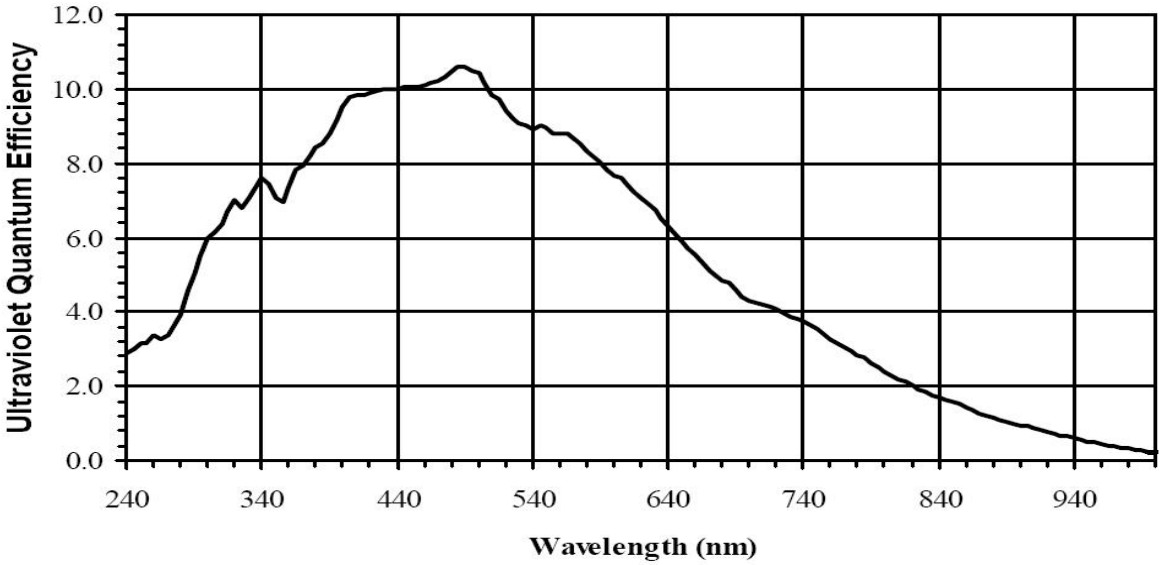


Figure 1.3 - Spectral response – UV quantum efficiency
(Measured without the cover glass)

Specifications	IPX-VGA120	IPX-VGA210
Active image pixels	640 (H) x 480 (V)	640 (H) x 480 (V)
Active image area	5.87 mm x 4.71 mm (0.231" x 0.185")	5.87 mm x 4.71 mm (0.231" x 0.185")
Pixel size	7.4 µm	7.4 µm
Video output	Digital, 8/10/12 bit, one output	Digital, 8/10/12 bit, one or two outputs
Tap reordering	No	No
Data clock	40.000 MHz	40.000 MHz
Camera interface	Base Camera Link	Base Camera Link
RS 232 interface	Yes	Yes
Resolution	640 x 480 pixels	640 x 480 pixels
Nominal frame rate	120 fps	210 fps
Maximum frame rate	up to 2200 fps	up to 2600 fps
S/N ratio	60 dB	60 dB
Binning	1 x 1, 2 x 2	1 x 1, 2 x 2
Area of interest	2 x 2 pixels min. size	2 x 2 pixels min. size
Mirror image	Yes, single output only	Yes, single output only
Negative image	No	No
Test image	Yes	Yes
Shutter speed	1/100000 to 1/100 sec	1/100000 to 1/100 sec
Long integration	Up to 10 sec	Up to 10 sec
Gamma correction	G=1.0, G=0.45	G=1.0, G=0.45
Black level offset	256 levels per output	256 levels per output
Video gain	6 to 40 dB per output	6 to 40 dB per output
Gain resolution	0.0351 dB/step, 1024 steps	0.0351 dB/step, 1024 steps
Hardware trigger	Asynchronous, active HIGH, optically isolated	Asynchronous, active HIGH, optically isolated
Software trigger	Asynchronous, frame-grabber via CC1	Asynchronous, frame-grabber via CC1
Trigger modes	Programmable exposure	Programmable exposure
Strobe output	Active HIGH	Active HIGH
Camera housing	Solid, anodized aluminum	Solid, anodized aluminum
Size (W x H x L) mm	67 x 67 x 41	67 x 67 x 41
Weight	280 g	280 g
Min. illumination	1.0 Lux, f=1.4	1.0 Lux, f=1.4
Lens Mount	C mount, 1/3" format	C mount, 1/3" format
Power input range	10 V to 15 V DC	10 V to 15 V DC
Power consumption	4.0 W	4.2 W
Upgradeable firmware	No	No
Upgradeable software	No	No
Environmental	Operating: -5 to 50 C Storage: -10 to 65 C	Operating: -5 to 50 C Storage: -10 to 65 C
Relative humidity	80% non-condensing	80% non-condensing

Table 1.1 - Camera Specifications

Specifications	IPX-1M48	IPX-2M30	IPX-2M30H
Active image pixels	1004 (H) x 1004 (V)	1600 (H) x 1200 (V)	1920 (H) x 1080 (V)
Active image area	8.90 mm x 8.20 mm (0.350" x 0.320")	13.38 mm x 9.52 mm (0.527" x 0.375")	15.90 mm x 8.61 mm (0.626" x 0.339")
Pixel size	7.4 µm	7.4 µm	7.4 µm
Video output	Digital, 8/10/12 bit, one output	Digital, 8/10/12 bit, one output	Digital, 8/10/12 bit, one or two outputs
Tap reordering	No	No	No
Data clock	40.000 MHz	40.000 MHz	40.000 MHz
Camera interface	Base Camera Link	Base Camera Link	Base Camera Link
RS 232 interface	Yes	Yes	Yes
Resolution	1004 x 1004 pixels	1600 x 1200 pixels	1920 x 1080 pixels
Nominal frame rate	48 fps	33 fps	33 fps
Maximum frame rate	up to 140 fps	up to 60 fps	up to 200 fps
S/N ratio	60 dB	60 dB	60 dB
Binning	1 x 1, 2 x 2	1 x 1, 2 x 2	1 x 1, 2 x 2
Area of interest	2 x 2 pixels min. size	2 x 2 pixels min. size	2 x 2 pixels min. size
Mirror image	Yes, single output only	Yes, single output only	Yes, single output only
Negative image	No	No	No
Test image	Yes	Yes	Yes
Shutter speed	1/50000 to 1/30 sec	1/40000 to 1/15 sec	1/35000 to 1/15 sec
Long integration	Up to 10 sec	Up to 10 sec	Up to 10 sec
Gamma correction	G=1.0, G=0.45	G=1.0, G=0.45	G=1.0, G=0.45
Black level offset	256 levels per output	256 levels per output	256 levels per output
Video gain	0 to 36 dB per output	6 to 40 dB per output	6 to 40 dB per output
Gain resolution	0.0351 dB/step, 1024 steps	0.0351 dB/step, 1024 steps	0.0351 dB/step, 1024 steps
Hardware trigger	Asynchronous, active HIGH, optically isolated	Asynchronous, active HIGH, optically isolated	Asynchronous, active HIGH, optically isolated
Software trigger	Asynchronous, frame-grabber via CC1	Asynchronous, frame-grabber via CC1	Asynchronous, frame-grabber via CC1
Trigger modes	Programmable exposure	Programmable exposure	Programmable exposure
Strobe output	Active HIGH	Active HIGH	Active HIGH
Camera housing	Solid, anodized aluminum	Solid, anodized aluminum	Solid, anodized aluminum
Size (W x H x L)	67 x 67 x 41	67 x 67 x 47	67 x 67 x 47
Weight	280 g	310 g	310 g
Min. illumination	1.0 Lux, f=1.4	1.0 Lux, f=1.4	1.0 Lux, f=1.4
Lens Mount	C mount, 2/3" format	C mount, 1" format	C mount, 1" format
Power input range	10 V to 15 V DC	10 V to 15 V DC	10 V to 15 V DC
Power consumption	3.6 W	4.8 W	4.8 W
Upgradeable firmware	No	No	No
Upgradeable software	No	No	No
Environmental	Operating: -5 to 50 C Storage: -10 to 65 C	Operating: -5 to 50 C Storage: -10 to 65 C	Operating: -5 to 50 C Storage: -10 to 65 C
Relative humidity	80% non-condensing	80% non-condensing	80% non-condensing

Table 1.1 - Camera Specifications (cont.)

Specifications	IPX-4M15	IPX-11M5
Active image pixels	2048 (H) x 2048 (V)	4000 (H) x 2672 (V)
Active image area	16.67 mm x 16.05 mm (0.656" x 0.632")	37.25 mm x 25.70 mm (1.466" x 1.012")
Pixel size	7.4 µm	9.0 µm
Video output	Digital, 8/10/12 bit, one output	Digital, 8/10/12 bit, one output
Tap reordering	No	No
Data clock	40.000 MHz	28.000 MHz
Camera interface	Base Camera Link	Base Camera Link
RS 232 interface	Yes	Yes
Resolution	2048 x 2048 pixels	4000 x 2672 pixels
Nominal frame rate	15 fps	5 fps
Maximum frame rate	up to 115 fps	up to 49 fps
S/N ratio	60 dB	60 dB
Binning	1 x 1, 2 x 2	1 x 1, 2 x 2
Area of interest	2 x 2 pixels min. size	2 x 2 pixels min. size
Mirror image	Yes, single output only	Yes, single output only
Negative image	No	No
Test image	Yes	Yes
Shutter speed	1/30000 sec to 1/7 sec	1/12000 sec to 1/3 sec
Long integration	Up to 10 sec	Up to 10 sec
Gamma correction	G=1.0, G=0.45	G=1.0, G=0.45
Black level offset	256 levels per output	256 levels per output
Video gain	6 to 40 dB per output	6 to 40 dB per output
Gain resolution	0.0351 dB/step, 1024 steps	0.0351 dB/step, 1024 steps
Hardware trigger	Asynchronous, active HIGH, optically isolated	Asynchronous, active HIGH, optically isolated
Software trigger	Asynchronous, frame-grabber via CC1	Asynchronous, frame-grabber via CC1
Trigger modes	Programmable exposure	Programmable exposure
Strobe output	Active HIGH	Active HIGH
Camera housing	Solid, anodized aluminum	Solid, anodized aluminum
Size (W x H x L)	67 x 67 x 47	67 x 67 x 47
Weight	360 g	390 g
Min. illumination	1.0 Lux, f=1.4	1.0 Lux, f=1.4
Lens Mount	F mount, 22mm format	F mount, 43mm format
Power input range	10 V to 15 V DC	10 V to 15 V DC
Power consumption	5.2 W	6.0 W
Upgradeable firmware	No	No
Upgradeable software	No	No
Environmental	Operating: -5 to 50 C Storage: -10 to 65 C	Operating: -5 to 50 C Storage: -10 to 65 C
Relative humidity	80% non-condensing	80% non-condensing

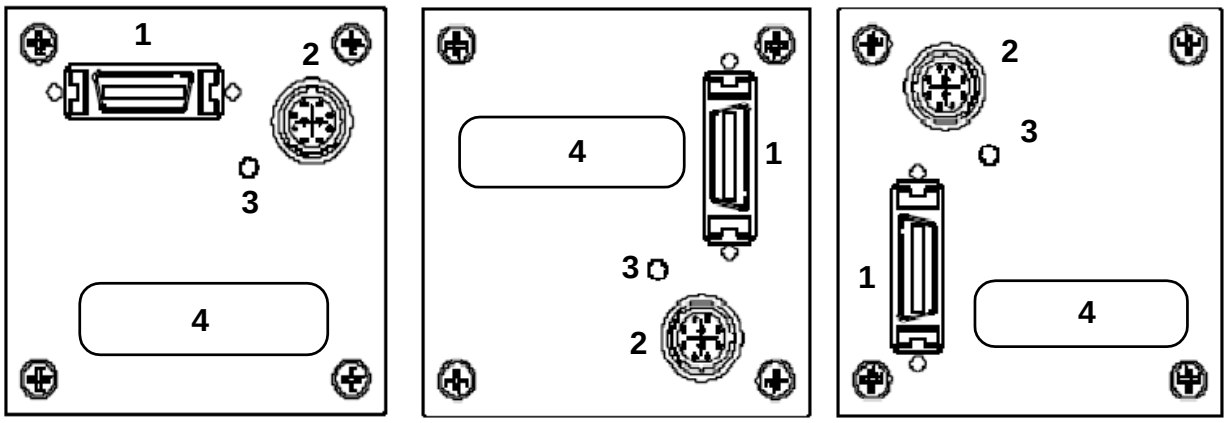
Table 1.1 - Camera Specifications (cont.)

1.4 CAMERA CONNECTIVITY

1.4.1 General Description

The interface between the IPX camera and outside equipment is done via two connectors and one LED, located on the back panel of the camera – Figure 1.4a.

1. Camera output – standard base Camera Link provides data, sync, control, and serial interface.
2. Power Connector – provides power and I/O interface.
3. Status LED – indicates the status of the camera – refer to Status LED section.
4. Serial Number – shows camera model and serial number.



IPX-VGA / 2M30 / 2M30H / 11M5 **IPX-1M48** **IPX-4M15**

Figure 1.4a – New IPX Camera Back Panel (sold after March 1, 2005)

CAUTION NOTE

1. Old IMPX and MDC cameras sold prior to March 1, 2005 have back panel shown on Figure 1.4b.

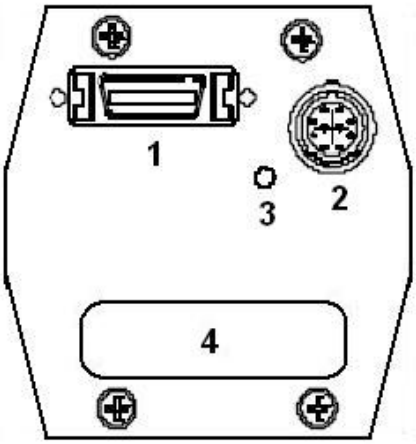


Figure 1.4b – Old IPX and MDC Camera Back Panel

1.4.2 Power Supply

A universal desktop power supply adapter, providing +12 VDC, +/- 5%, and up to 1.5A constant DC current, is available from Imperx for the IPX cameras. The operating input voltage ranges from 90 to 240 VAC.

CAUTION NOTE

1. It is strongly recommended that you do not use an adapter other than the one that is available from Imperx for the camera!

1.4.3 Camera Output Connector

Camera data output is compliant with base Camera Link standard and includes 24 data bits, 3 sync signals (LVAL, FVAL and DVAL), 1 reference clock, 1 external input trigger CC1 and a bi-directional serial interface. The output connector is shown in Figure 1.5, and the corresponding signal mapping in Table 1.2.

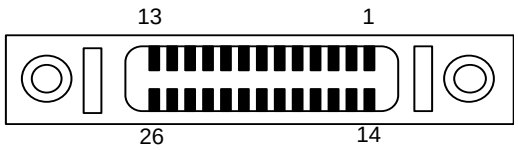


Figure 1.5 - Camera Output Connector

Pin Assignment

Cable Name	Pin	CL Signal	Type	Description
Inner Shield	**1**	Inner Shield	Ground	Cable Shield
Inner Shield	**14**	Inner Shield	Ground	Cable Shield
- PAIR 1	**2**	- X 0	LVDS - Out	Camera Link Channel Tx
+ PAIR 1	**15**	+ X 0	LVDS - Out	Camera Link Channel Tx
- PAIR 2	**3**	- X 1	LVDS - Out	Camera Link Channel Tx
+ PAIR 2	**16**	+ X 1	LVDS - Out	Camera Link Channel Tx
- PAIR 3	**4**	- X 2	LVDS - Out	Camera Link Channel Tx
+ PAIR 3	**17**	+ X 2	LVDS - Out	Camera Link Channel Tx
- PAIR 4	**5**	- X CLK	LVDS - Out	Camera Link Clock Tx
+ PAIR 4	**18**	+ X CLK	LVDS - Out	Camera Link Clock Tx
- PAIR 5	**6**	- X 3	LVDS - Out	Camera Link Channel Tx
+ PAIR 5	**19**	+ X 3	LVDS - Out	Camera Link Channel Tx
+ PAIR 6	**7**	+ SerTC	LVDS - In	Serial Data Receiver
- PAIR 6	**20**	- SerTC	LVDS - In	Serial Data Receiver
- PAIR 7	**8**	- SerTFG	LVDS - Out	Serial Data Transmitter
+ PAIR 7	**21**	+ SerTFG	LVDS - Out	Serial Data Transmitter
- PAIR 8	**9**	- CC 1	LVDS - In	Software External Trigger
+ PAIR 8	**22**	+ CC 1	LVDS - In	Software External Trigger
+ PAIR 9	**10**	N/C	N/C	N/C
- PAIR 9	**23**	N/C	N/C	N/C
- PAIR 10	**11**	N/C	N/C	N/C
+ PAIR 10	**24**	N/C	N/C	N/C
+ PAIR 11	**12**	N/C	N/C	N/C
- PAIR 11	**25**	N/C	N/C	N/C
Inner Shield	**13**	Inner Shield	Ground	Cable Shield
Inner Shield	**26**	Inner Shield	Ground	Cable Shield

Table 1.2 - Camera Output Connector – Signal Mapping

The bit assignment corresponding to the base configuration is shown in the following table.

Port	Port/bit	8-bits Tap 1, 2	10-bits Tap1,2	12-bits Tap 1, 2
DATA 0	Port A0	A0	A0	A0
DATA 1	Port A1	A1	A1	A1
DATA 2	Port A2	A2	A2	A2
DATA 3	Port A3	A3	A3	A3
DATA 4	Port A4	A4	A4	A4
DATA 5	Port A5	A5	A5	A5
DATA 6	Port A6	A6	A6	A6
DATA 7	Port A7	A7	A7	A7
DATA 8	Port B0	B0	A8	A8
DATA 9	Port B1	B1	A9	A9
DATA 10	Port B2	B2	N/C	A10
DATA 11	Port B3	B3	N/C	A11
DATA 12	Port B4	B4	B8	B8
DATA 13	Port B5	B5	B9	B9
DATA 14	Port B6	B6	N/C	B10
DATA 15	Port B7	B7	N/C	B11
DATA 16	Port C0	N/C	B0	B0
DATA 17	Port C1	N/C	B1	B1
DATA 18	Port C2	N/C	B2	B2
DATA 19	Port C3	N/C	B3	B3
DATA 20	Port C4	N/C	B4	B4
DATA 21	Port C5	N/C	B5	B5
DATA 22	Port C6	N/C	B6	B6
DATA 23	Port C7	N/C	B7	B7
ENABLE 0	LVAL	LVAL	LVAL	LVAL
ENABLE 1	FVAL	FVAL	FVAL	FVAL
ENABLE 2	DVAL	DVAL	DVAL	DVAL
ENABLE 3	N/C	N/C	N/C	N/C
CONTROL 0	CC 1	CC 1	CC 1	CC 1
CONTROL 1	N/C	N/C	N/C	N/C
CONTROL 2	N/C	N/C	N/C	N/C
CONTROL 3	N/C	N/C	N/C	N/C

Table 1.3 - Base Camera Link bit assignment

1.4.4 Camera Power Connector

The power and all external input/output signals are supplied to the camera via the camera power connector shown in Figure 1.6. The corresponding pin mapping is shown in Table 1.4. The connector is a HIROSE type miniature locking receptacle #HR10A-10R-10PB.

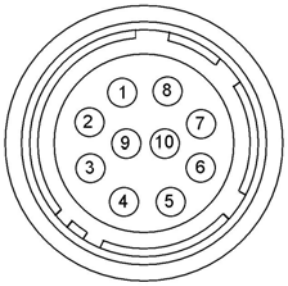


Figure 1.6 - Camera Power Connector (viewed from rear)

Pin	Signal	Type	Description
1	Trigger In -	TTL - Input	External Trigger Input
2	Trigger In +	TTL - Input	External Trigger Input
3	GND	Power - Input	Power Ground Return
4	GND	Power - Input	Power Ground Return
5	+ 12 V	Power - Input	+ 12 V Power Supply
6	+ 12 V	Power - Input	+ 12 V Power Supply
7	Strobe Out -	TTL - Output	Strobe Light Sync Pulse
8	Strobe Out +	TTL - Output	Strobe Light Sync Pulse
9	Reserve	-	Do not use
10	Reserve	-	Do not use

Table 1.4 - Camera Power Connector Pin Mapping

The camera is shipped with a power cable which terminates in a HIROSE plug #HR10A-10P-10S, and has two small BNC pig-tail cables for the external trigger input (black) and strobe output (white). The corresponding BNC connector pin mapping is shown below – Table 1.5a.

Pin	Signal	Cable color	Description
Shield	Trigger In -	BNC Black	External Trigger Input
Signal	Trigger In +		External Trigger Input
Shield	Strobe Out -	BNC White	Strobe Light Sync Pulse
Signal	Strobe Out +		Strobe Light Sync Pulse

Table 1.5a - BNC Connectors Pin Mapping

CAUTION NOTE

1. Old IPX and MDC camera shipped prior to March 1, 2005, come with a power cable which terminates in a HIROSE plug #HR10A-10R-10P, and have a small pig-tail cable ending with 4 pin interface connector for the external trigger input and strobe output. The I/O interface connector is shown in Figure 1.7, and the corresponding pin mapping in Table 1.5b.

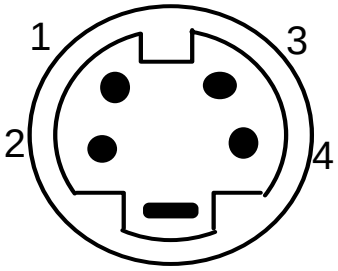


Figure 1.7. I/O Cable Interface – Old Connector.

Pin	Signal	Description
1	Trigger In -	External Trigger Input
2	Trigger In +	External Trigger Input
3	Strobe Out +	Strobe Light Sync Pulse
4	Strobe Out -	Strobe Light Sync Pulse

Table 1.5b – I/O Interface Connector - Pin Mapping

1.5 MECHANICAL, OPTICAL and ENVIRONMENTAL

1.5.1 Mechanical – New IPX

IPX cameras sold after March 1, 2005 - the camera housing is manufactured using high quality anodized aluminum. For maximum flexibility the camera has eight 10-32 UNF mounting holes (two on each side), located towards the front. Figures 1.8 and 1.9 show the front and back view of the C-mount and F-mount cameras respectively. Figures 1.10 to 1.14 show the mechanical detail drawings of IPX-VGA, IPX-1M48, IPX-2M30/H, IPX-4M15 and IPX-11M5 respectively. All dimensions are in millimeters.

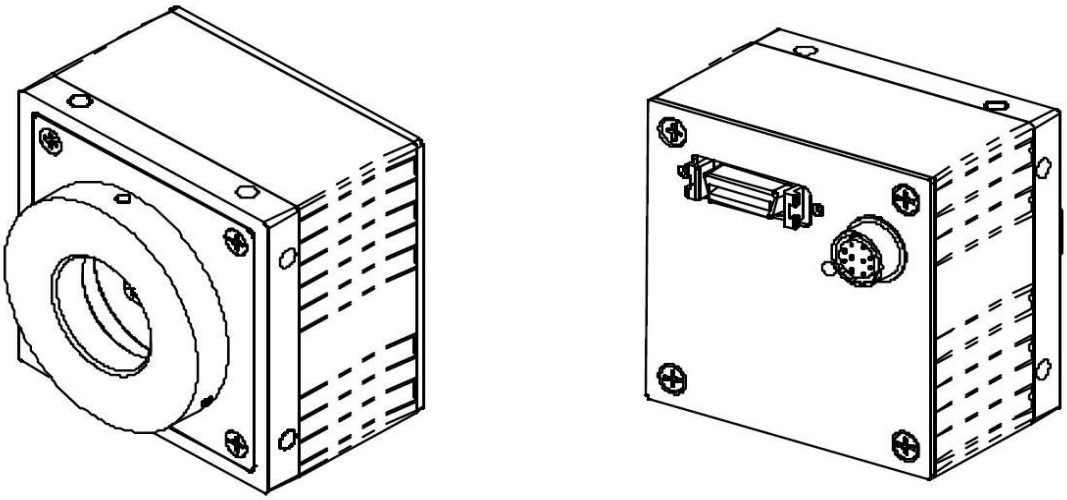


Figure 1.8 - C-mount cameras – IPX-VGA/1M48/2M30/2M30H

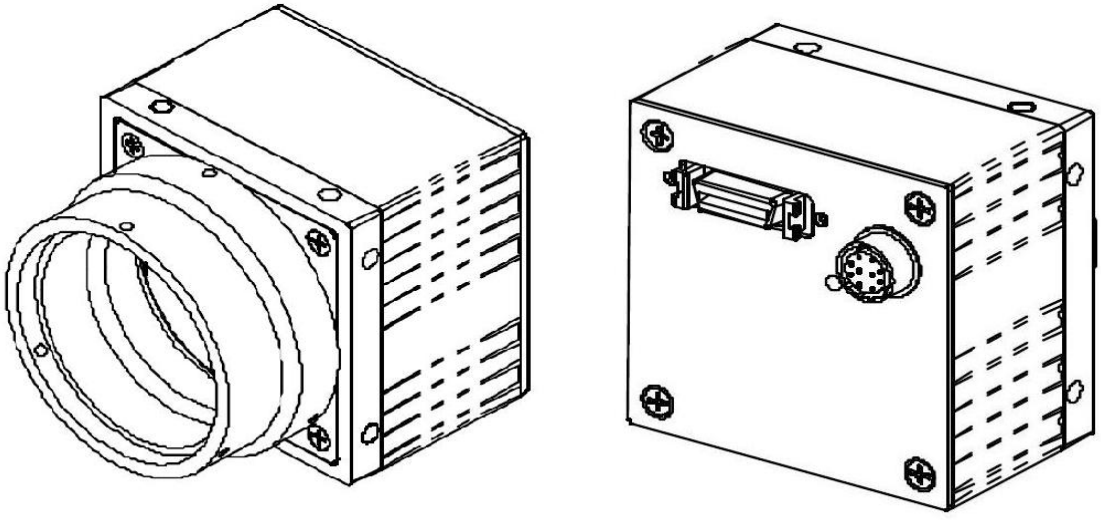


Figure 1.9 - F-mount cameras – IPX-4M15 and IPX-11M

IPX-VGA120 / VGA210
(Dimensional Drawings)

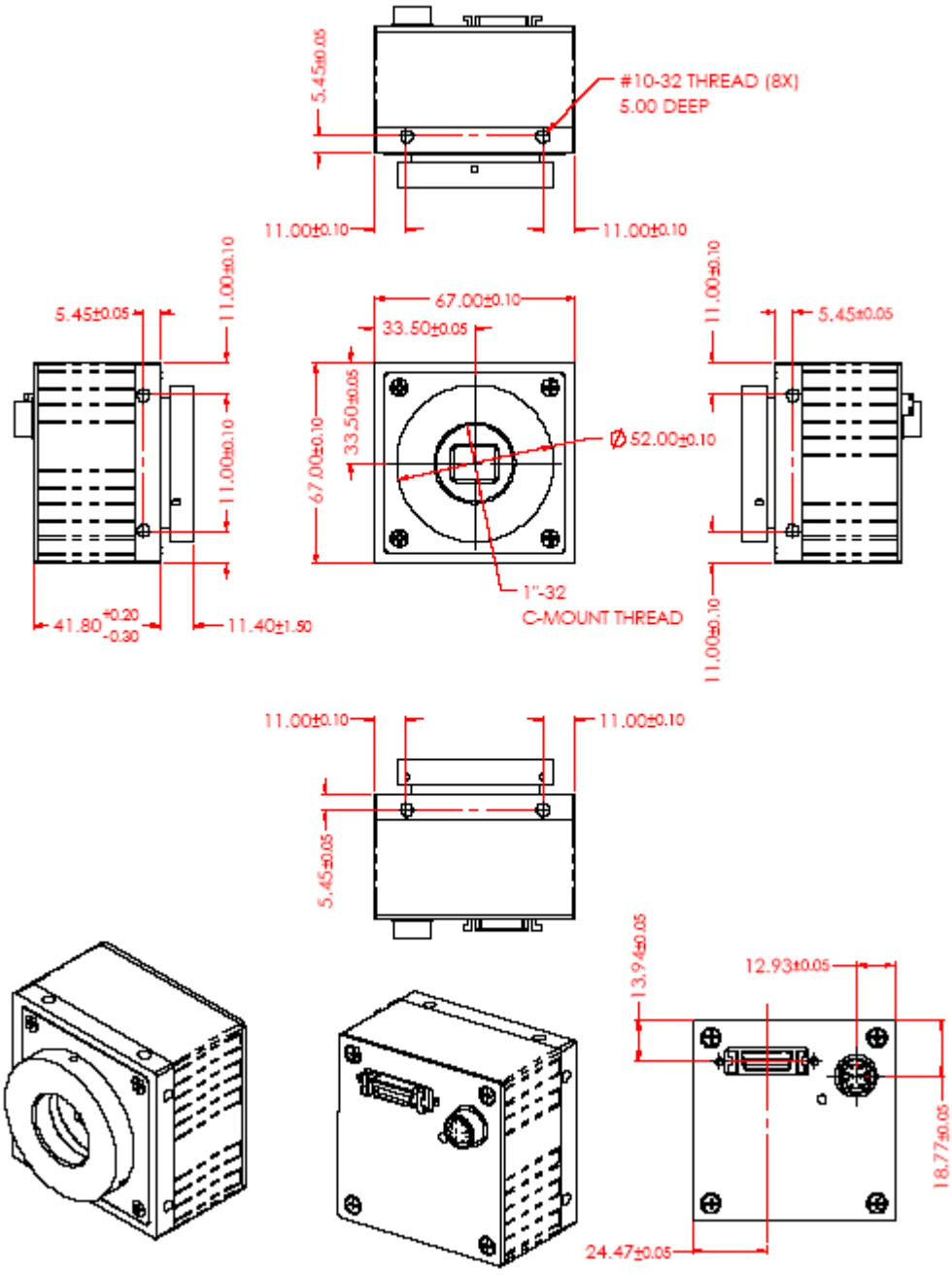


Figure 1.10 - IPX-VGA120 and IPX-VGA0210

IPX-1M48
(Dimensional Drawings)

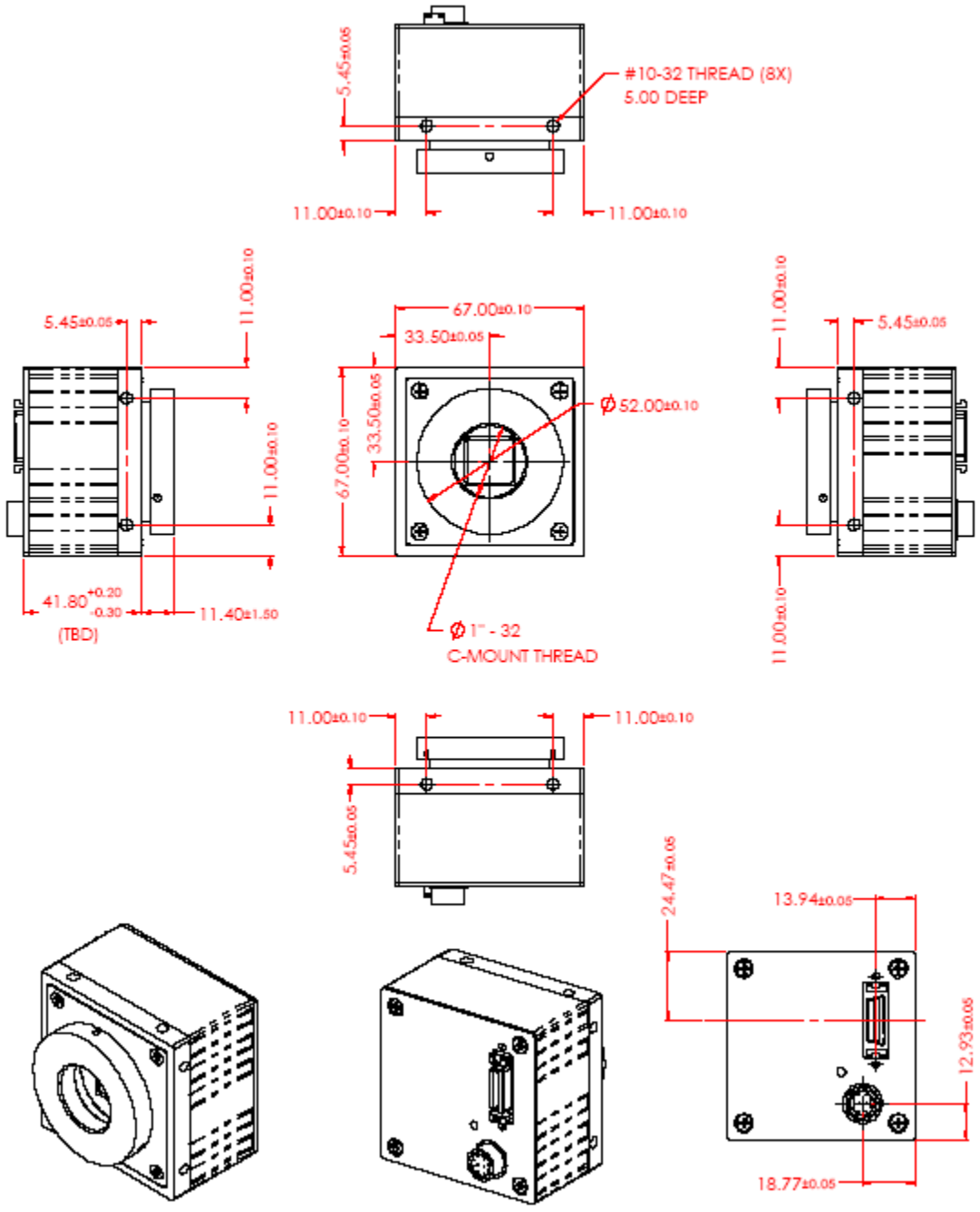


Figure 1.11 - IPX-1M48

IPX-2M30 / IPX-2M30H
(Dimensional Drawings)

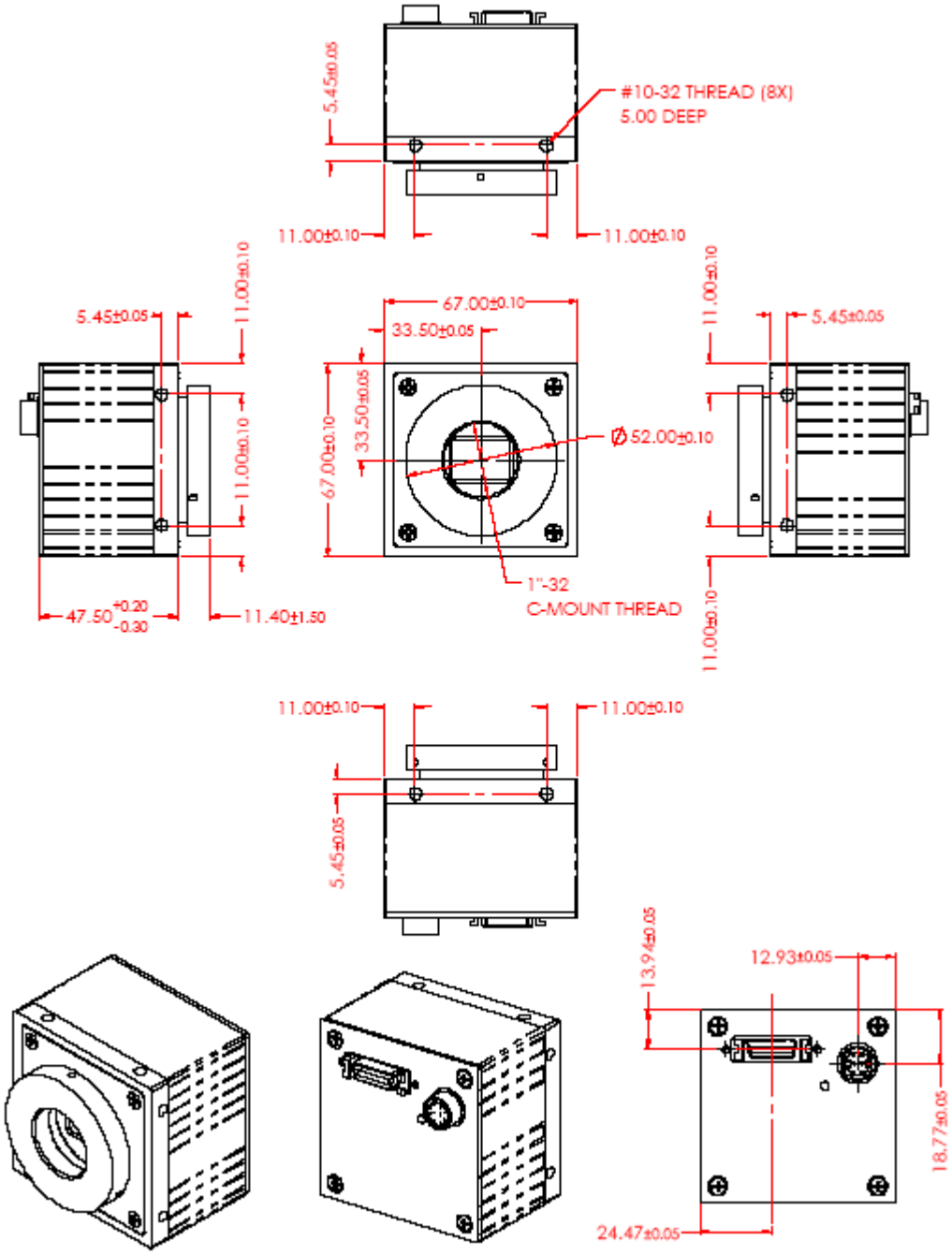


Figure 1.12 - IPX-2M30 and IPX-2M30H

IPX-4M15
(Dimensional Drawings)

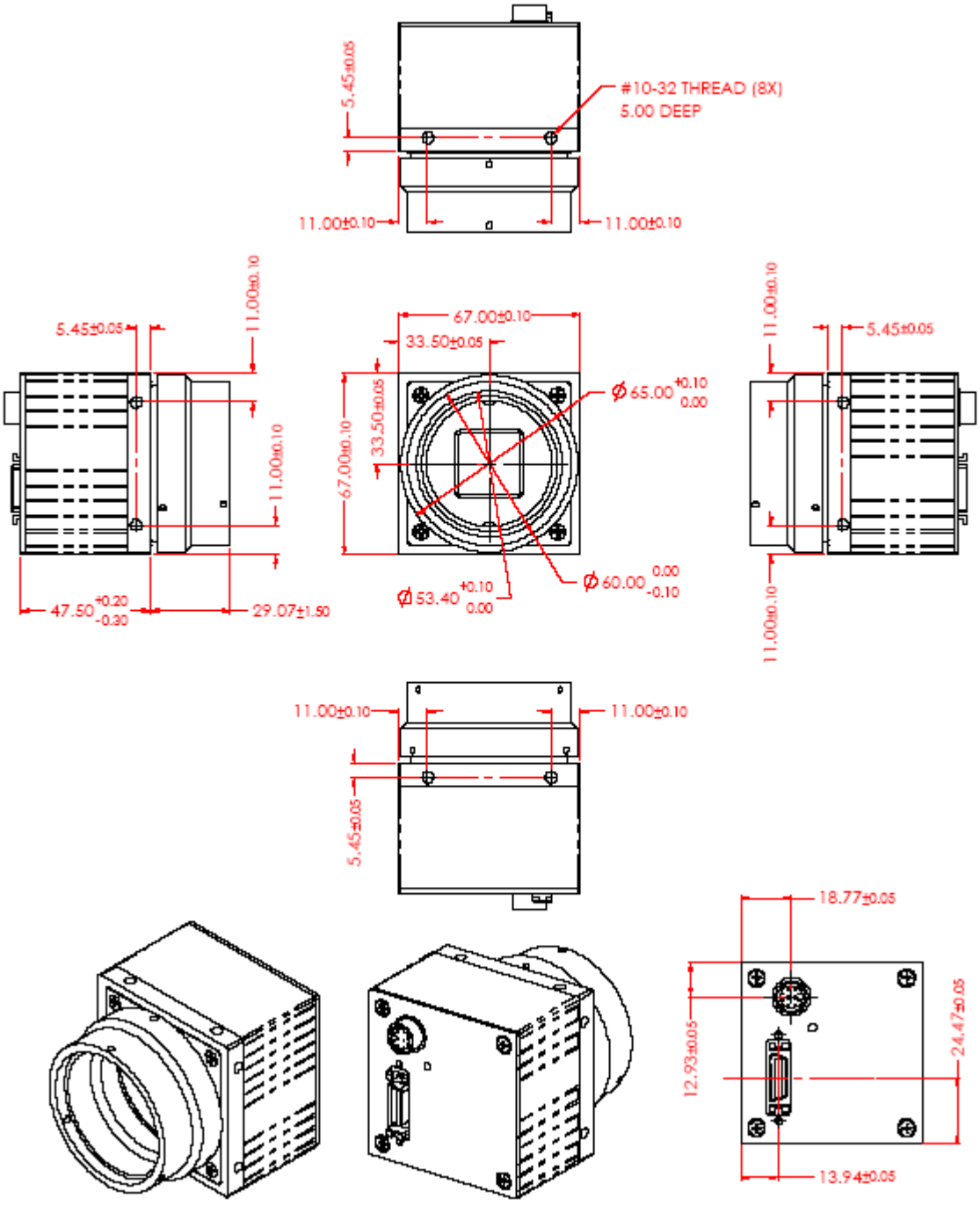


Figure 1.13 - IPX-4M15

IPX-11M5
(Dimensional Drawings)

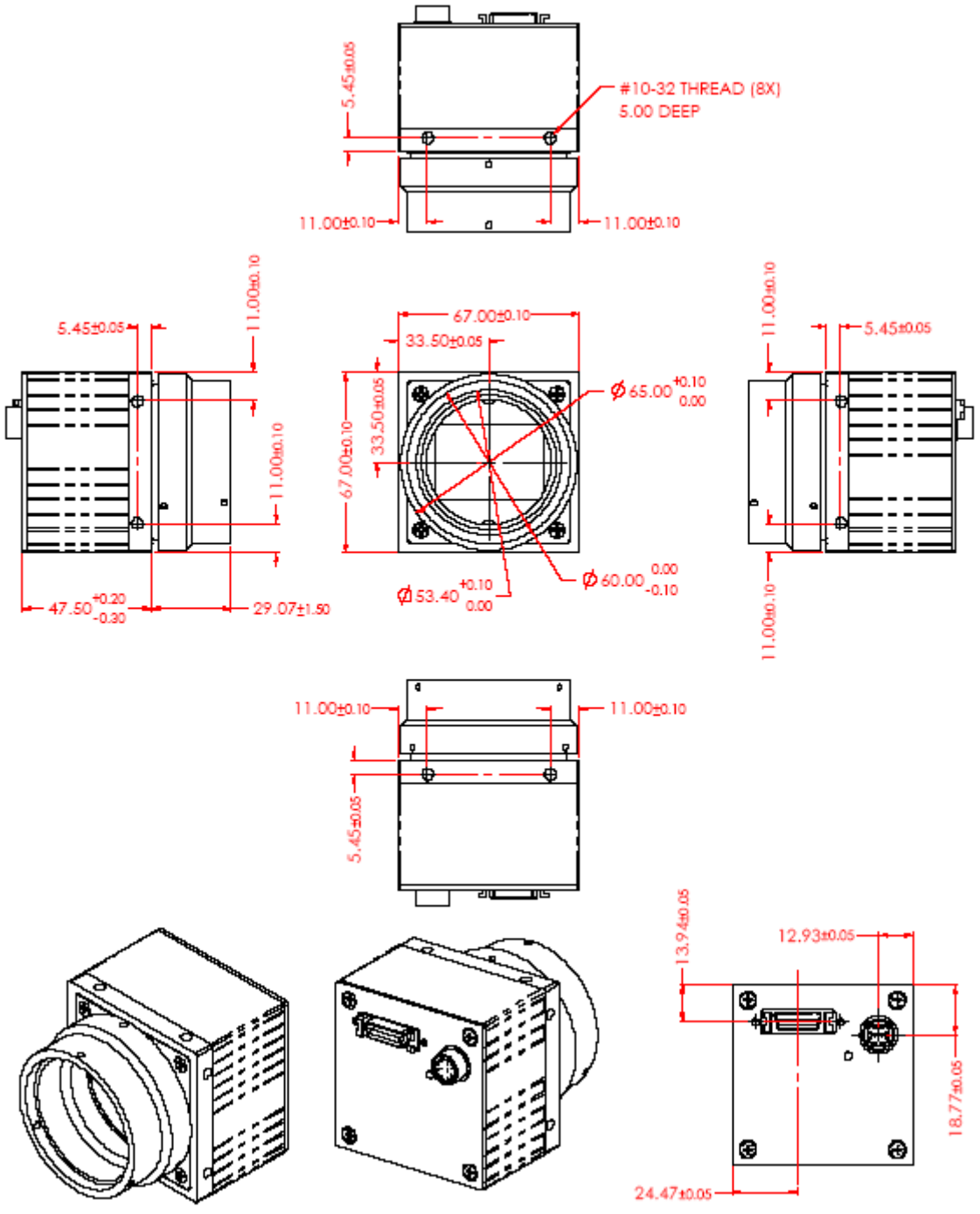


Figure 1.14 - IPX-11M5

1.5.2 Mechanical – Old IPX and MDC

IPX and MDC cameras sold prior to March 1, 2005 - the camera housing is manufactured using high quality anodized aluminum. For maximum flexibility the camera has one ¼ - 20 UNC tripod mounting hole on the bottom of the camera, located in the center, two 10-32 UNF holes on the top of the camera, located towards the back, and two 10-32 UNF holes on the bottom - located towards the back. Figures 1.15 to 1.18 show the mechanical detail drawings of IPX-VGA, IPX-1M48 (MDC1004), IPX-2M30 (MDC1600), IPX-2M30H (MDC1920), and IPX-4M15 (MDC2048) respectively. All dimensions are in millimeters [bracketed dimensions - in inches].

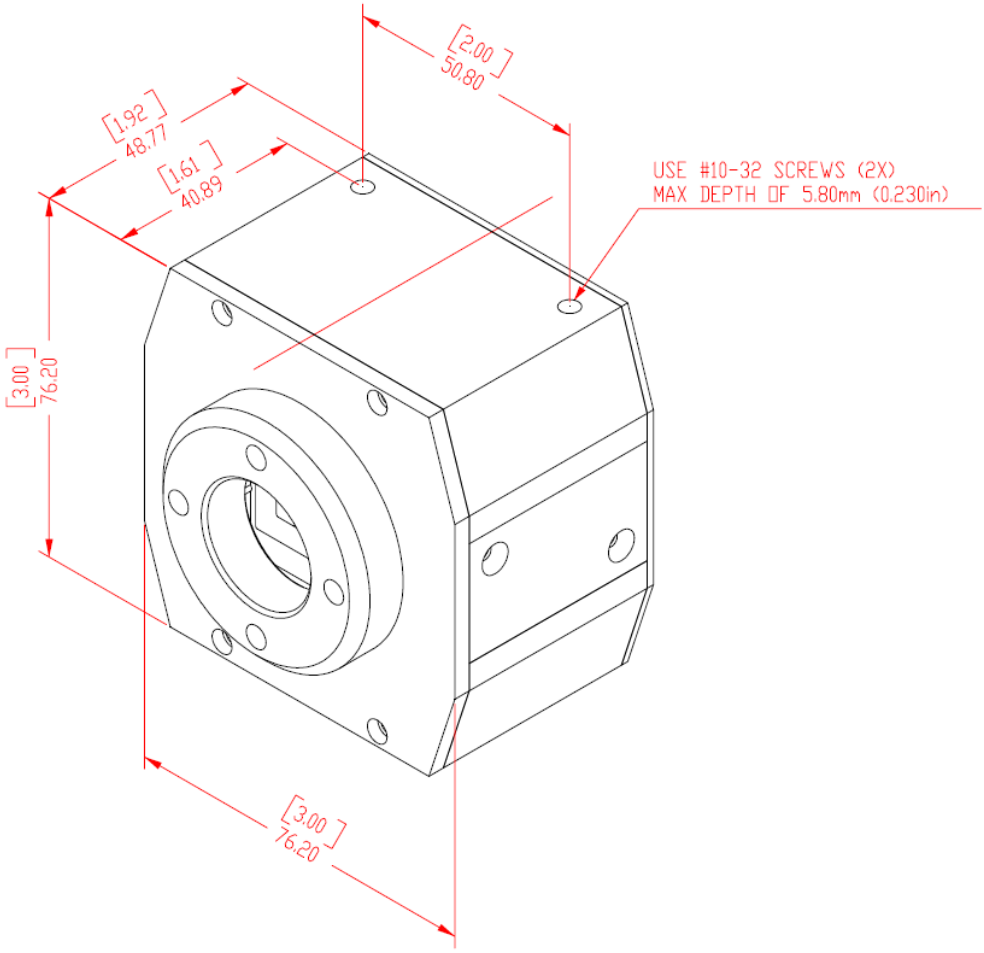


Figure 1.15. IPX-VGA, 2M30/H, 4M15, MDC1600, 1920, 2048 - Top View.

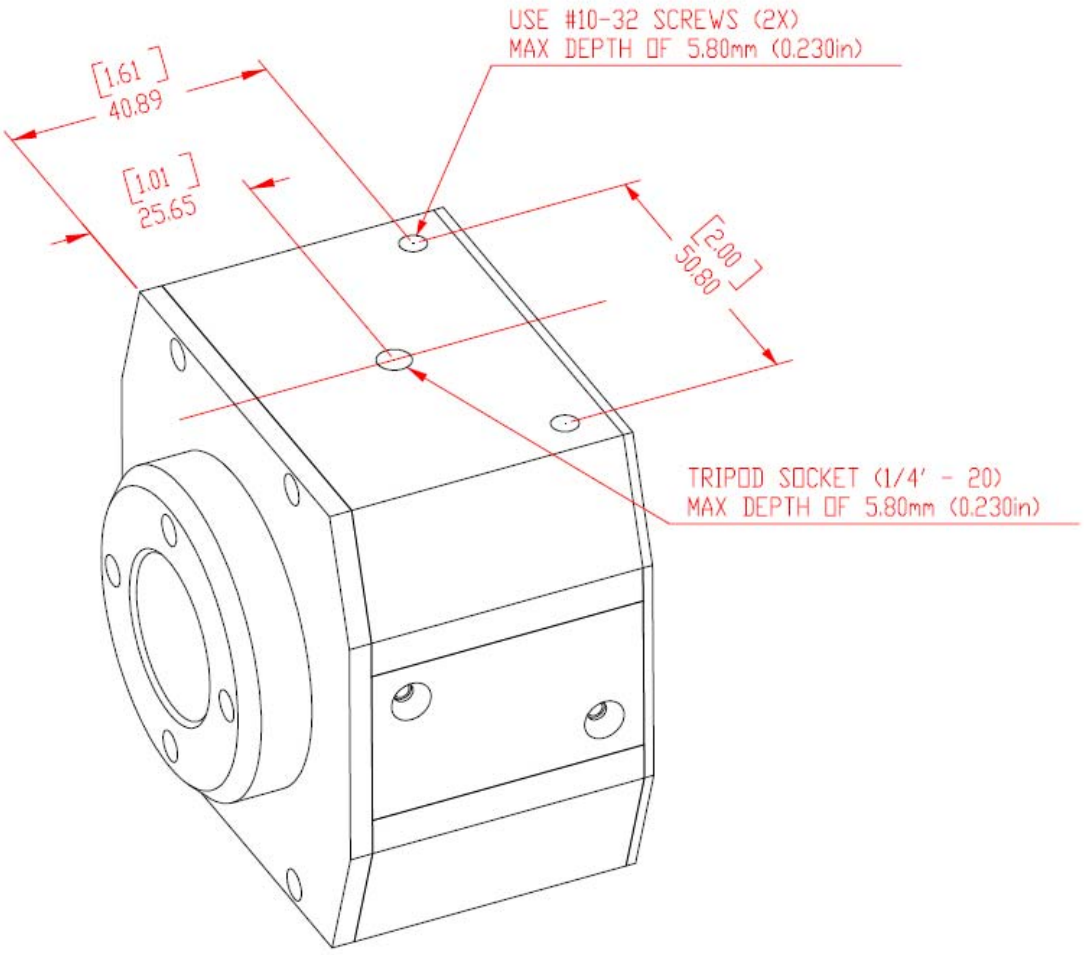


Figure 1.16. IPX-VGA, 2M30/H, 4M15, MDC1600, 1920, 2048 - Bottom View.

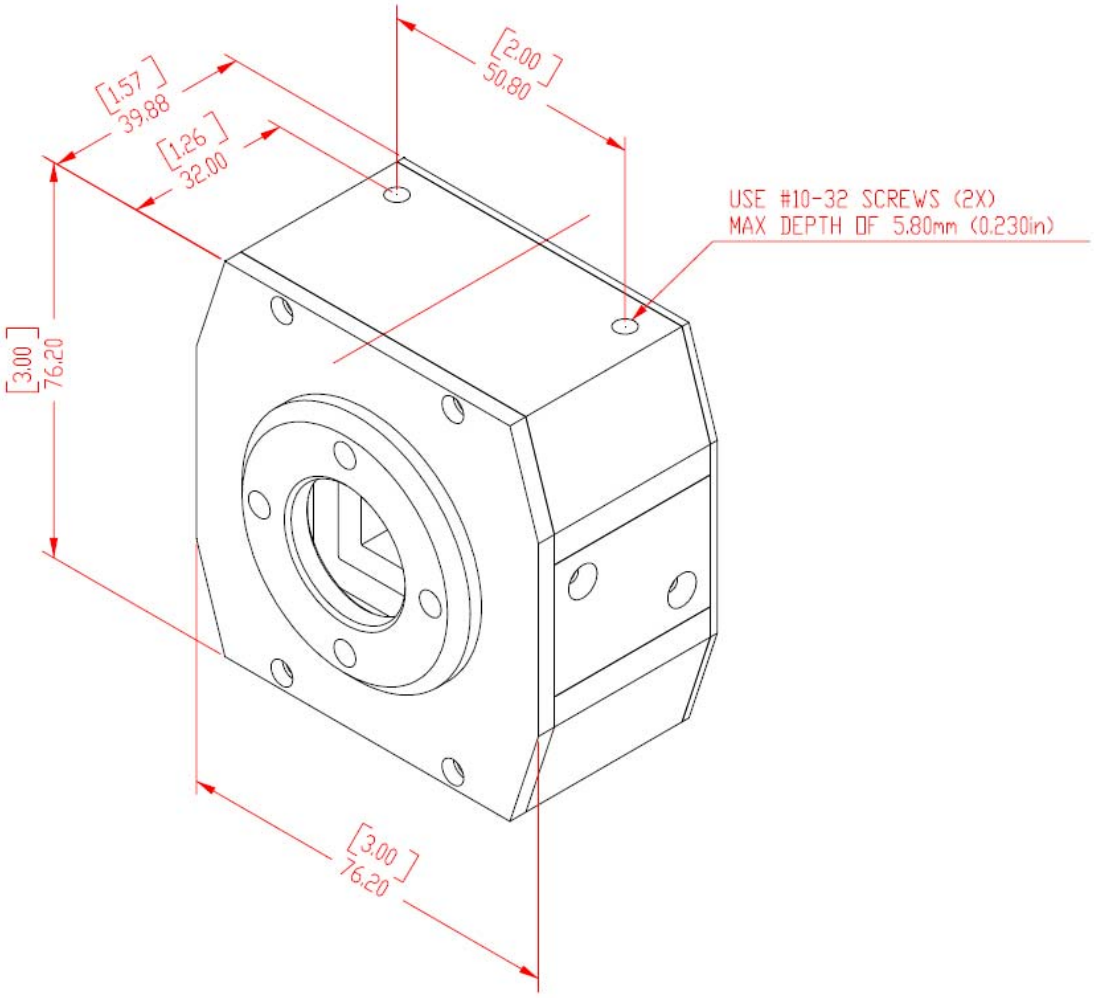


Figure 1.17. IPX-1M48 and MDC1004 - Top View.

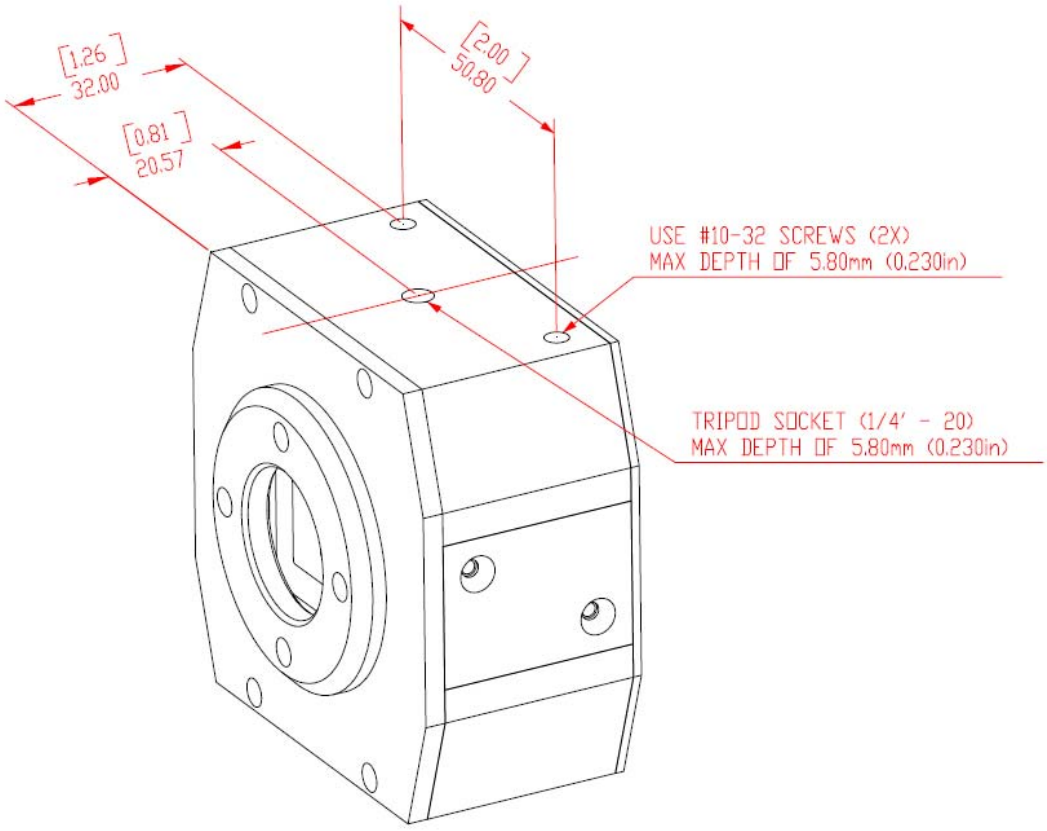


Figure 1.18. IPX-1M48 and MDC1004 - Bottom View.

1.5.3 Optical

The IPX-VGA, IPX-1M48, IPX-2M30 and IPX-2M30H cameras come with an adapter for C-mount lenses, which have a 17.5 mm back focal distance. The IPX-4M15 and IPX-11M5 cameras come with an adapter for F-mount lenses, which have a 46.5 mm back focal distance. An F-mount lens can be used with a C-mount camera via an F-mount to C-mount adapter, which can be purchased separately – refer to the Imperx web side for more information. The camera performance and signal to noise ratio depends on the illumination (amount of light) reaching the sensor and the exposure time. Always try to balance these two factors. Unnecessarily long exposure will increase the amount of noise and thus decrease the signal to noise ratio.

The camera is very sensitive in the IR spectral region. If necessary, an IR filter (1 mm thickness or less) can be inserted under the front lens bezel.

CAUTION NOTE

1. Avoid direct exposure to a high intensity light source (such as a laser beam). This may damage the camera optical sensor!
2. Avoid foreign particles on the surface of the imager.

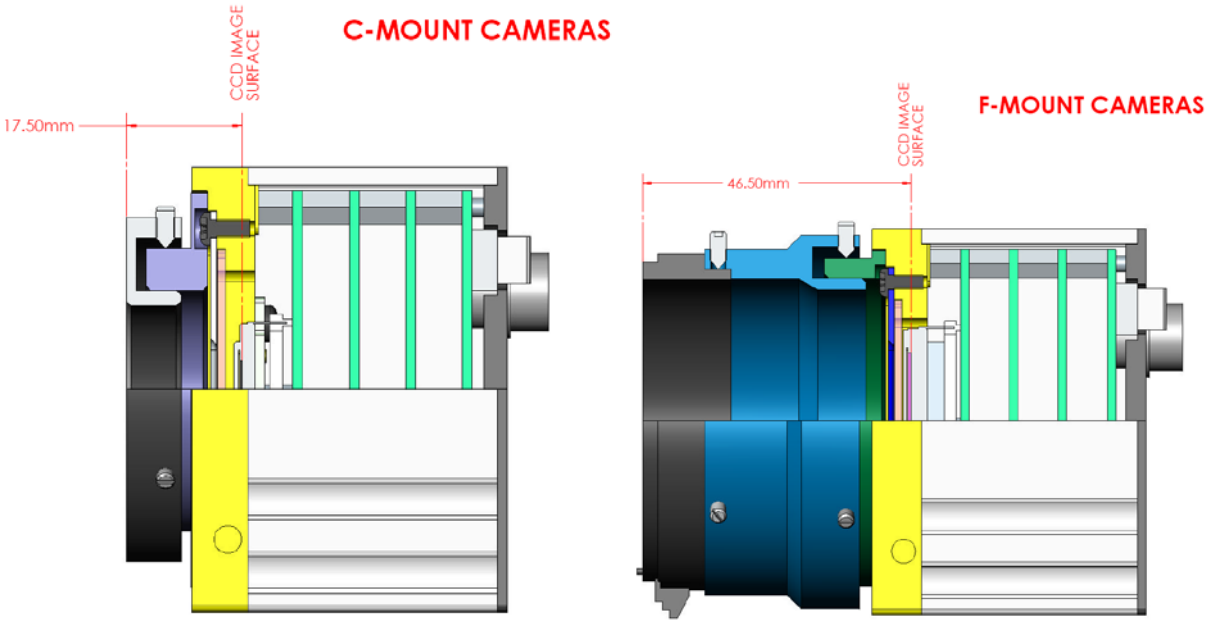


Figure 1.19 - C-mount and F-mount adapter

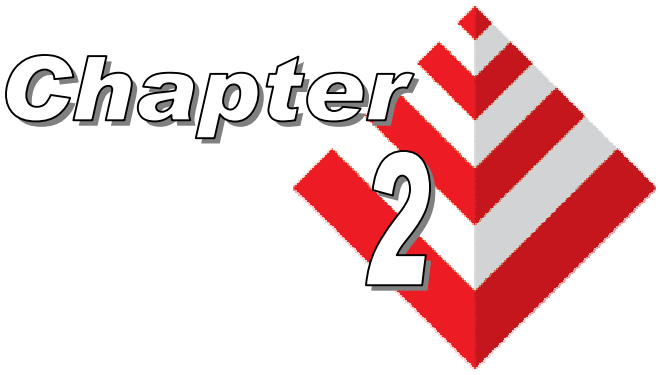
1.5.4 Environmental

The camera is designed to operate from -5^0 to 50^0 C in a dry environment. The relative humidity should not exceed 80% non-condensing. Always keep the camera as cool as possible. Always allow sufficient time for temperature equalization, if the camera was kept below 0^0 C!

The camera should be stored in a dry environment with the temperature ranging from -10^0 to $+ 65^0$ C.

CAUTION NOTE

1. Avoid direct exposure to moisture and liquids. The camera housing is not hermetically sealed and any exposure to liquids may damage the camera electronics!
2. Avoid operating in an environment without any air circulation, in close proximity to an intensive heat source, strong magnetic or electric fields.
3. Avoid touching or cleaning the front surface of the optical sensor. If the sensor needs to be cleaned, use soft lint free cloth and an optical cleaning fluid. Do not use methylated alcohol!



Camera Features

This chapter discusses the camera's features and their use.

2.1 RESOLUTION AND FRAME RATE

2.1.1 Single Output

When operating in the single output mode, all pixels are shifted out of the HCCD register towards the left video amplifier – Video L (Figure 2.1). The resulting image has a normal orientation, full resolution and a frame rate as shown in Table 2.1.

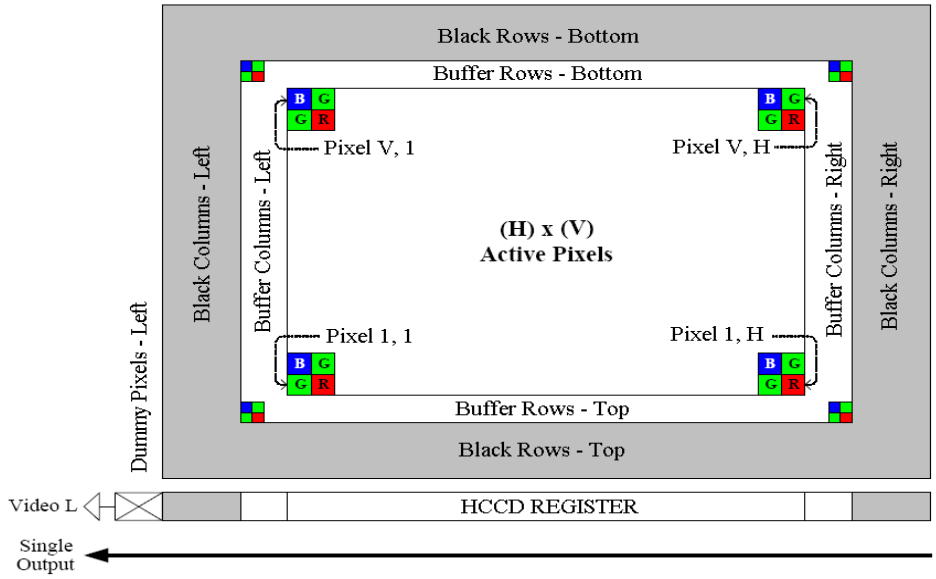


Figure 2.1 - Single Output Mode of Operation

Pixel Structure	IPX-VGA120	IPX-VGA210	IPX-1M48	IPX-2M30	IPX-2M30H	IPX-4M15	IPX-11M5
Black rows - top	4	4	4	2	4	10	16
Buffer rows - top	4	4	0	4	2	6	8
Active rows - (V)	**480**	**480**	**1004**	**1200**	**1080**	**2048**	**2672**
Buffer rows - bottom	4	4	0	4	2	8	8
Black rows - bottom	0	0	0	4	4	0	16
Dummy pixels - left	12	12	8	4	4	12	4
Black columns - left	24	24	12	16	28	28	20
Buffer columns - left	4	4	0	4	4	4	16
Active pixels - (H)	**640**	**640**	**1004**	**1600**	**1920**	**2048**	**4000**
Buffer columns - right	4	4	0	4	4	4	16
Black columns - right	24	24	12	16	28	28	20
Dummy pixels - right	12	12	8	4	4	12	4
Frame rate - single	120 fps	120 fps	30 fps	17 fps	17 fps	7.5 fps	2.5 fps
Frame rate - dual	n/a	210 fps	48 fps	33 fps	33 fps	15 fps	5 fps

Table 2.1 - Pixel Structure and Frame Rates

2.1.2 Dual Output

When operating in a dual output mode, the image is split in two equal parts, each side consisting of half of the horizontal pixels and the full vertical lines. The first (left) half of the pixels are shifted out of the HCCD register towards the left video amplifier – Video L, while the second (right) half of the pixels are shifted towards the right video amplifier – Video R (Figure 2.2). In the horizontal direction the first half of the image appears normal and the second half is left/right mirrored. To reconstruct the normal image the second half has to be mirrored in the frame grabber or software. Dual output is the default factory mode of operation – refer to the Configuration Memory section.

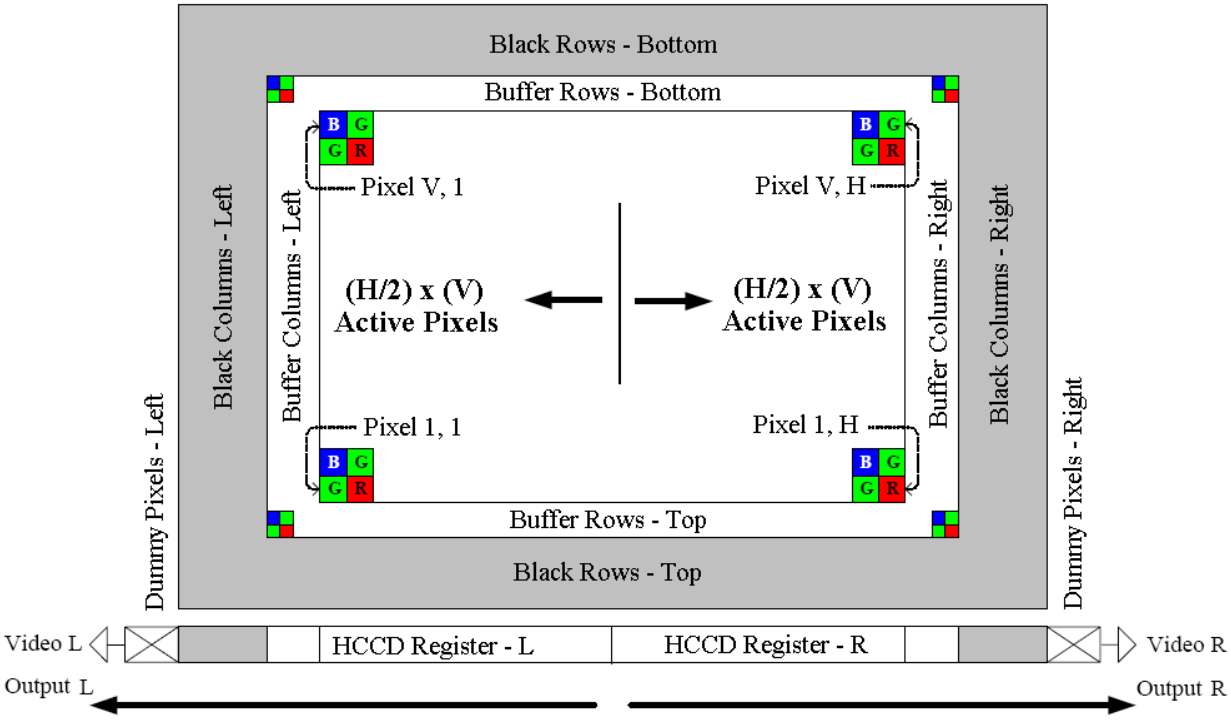


Figure 2.2 - Dual Output Mode of Operation.

For normal mode of operation the frame rate can be calculated using the following formula (Formula 1.1). Please note that the formula is not applicable if the shutter is enabled:

$$\text{Frame rate [fps]} = 1 / \text{exposure time [sec]} \qquad (1.1)$$

2.1.3 Timing Diagrams

IPX-VGA120, IPX-VGA210

In the single mode each line consists of 12 empty pixels (E1 – E12), followed by 24 masked pixels used for black reference (R1 – R24), followed by 4 buffer pixels (B1 – B4), followed by 640 active data pixels (D1 – D640), followed by 4 buffer pixels (B1 – B4), and followed by another 24 masked dark pixels (R1 – R24) – Figure 2.3. In dual mode each line consists of 12 empty pixels (E1 – E12), followed by 24 masked pixels used for black reference (R1 – R24), followed by 4 buffer pixels (B1 – B4), followed by 320 active data pixels – Figure 2.4. The data is sampled on the rising edge of the clock, and the LVAL (line valid) signal is active only during the active pixels. Each frame (for all modes) consists of 35.4 us vertical frame timing, followed by 4 masked dark lines (RL1 – RL4), followed by 4 buffer lines (B1 – B4), followed by 480 active lines (L1 – L480), and followed by 4 buffer lines (B1 – B4). During each frame the FVAL (frame valid) signal is active only during the active lines (L1 – L480) – Figure 2.5.

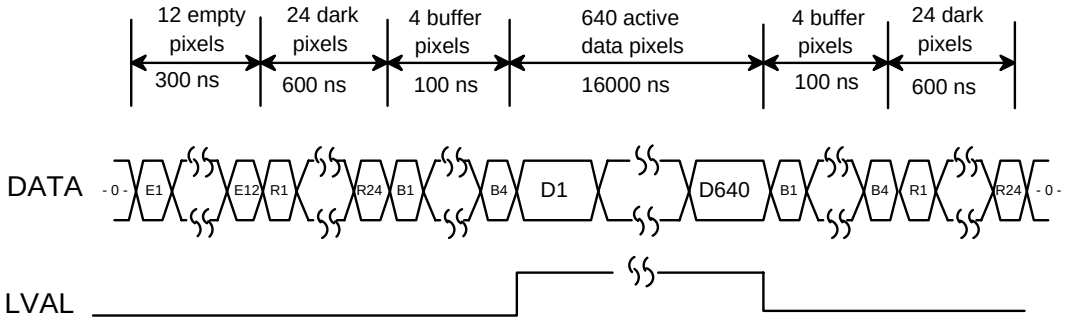


Figure 2.3 - Single Output Line Timing (IPX-VGA120/210)

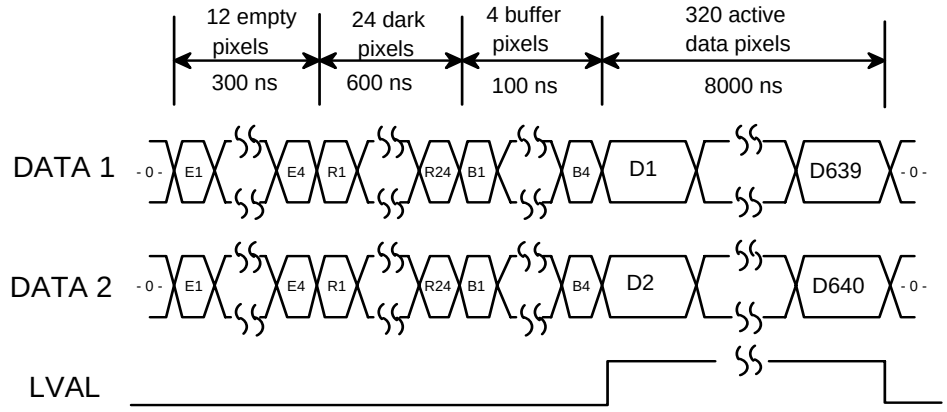
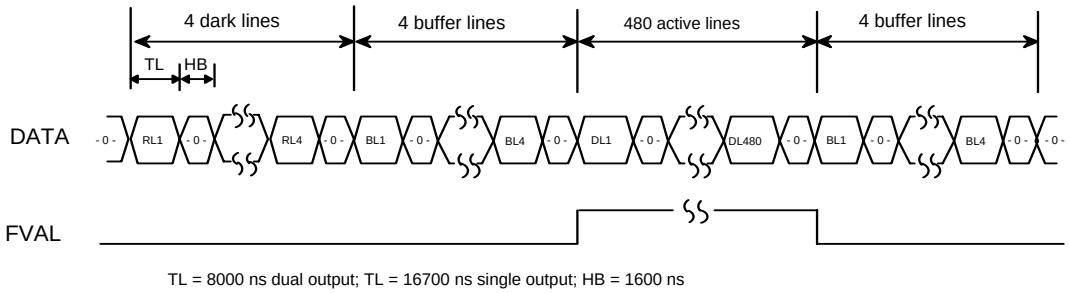


Figure 2.4 - Dual Output Line Timing (IPX-VGA120/210)



TL = 8000 ns dual output; TL = 16700 ns single output; HB = 1600 ns

Figure 2.5 - Single or Dual Output Frame Timing (IPX-VGA210)

IPX-VGA120: T_L = 18.38 µs for single, T_L = 9.7 µs for dual

IPX-VGA120: T_L = 18.4 µs

In the single mode, each line consists of 8 empty pixels (E1 – E8), followed by 12 masked pixels used for black (dark) reference (B1 – B12), followed by 1004 active pixels (D1 – D1004), and followed by another 12 masked pixels (B1 – B12) – Figure 2.6. In the dual mode, each line consists of 8 empty pixels (E1 – E8), followed by 12 masked pixels used for black (dark) reference (B1 – B12), and followed by 502 active pixels – Figure 2.7. The data is sampled on the rising edge of the clock, and the LVAL (line valid) signal is active only during the active pixels. Each frame (for all modes) consists of 61 us vertical frame timing, followed by 4 masked lines (BL1 – BL4), followed by 1004 active lines (L1 – L1004). During each frame the FVAL (frame valid) signal is active only during the active lines (L1 – L1004) – Figure 2.8.

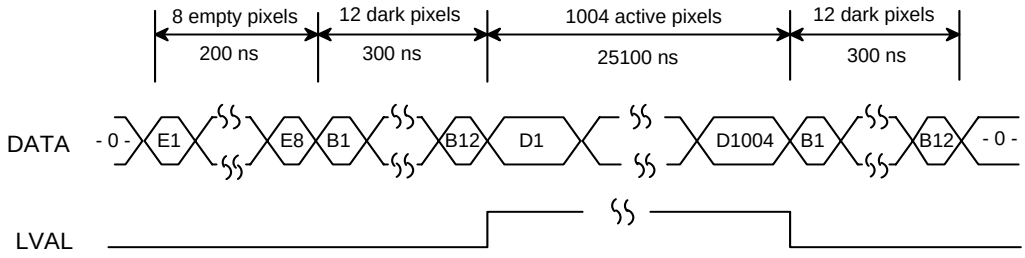


Figure 2.6 - Single Output Line Timing (IPX-1M48)

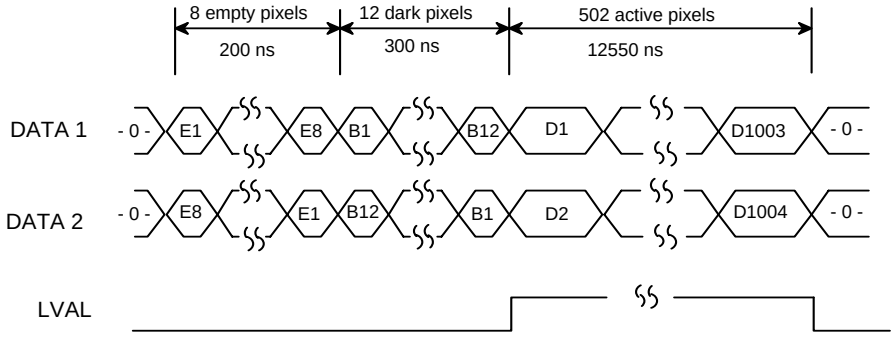
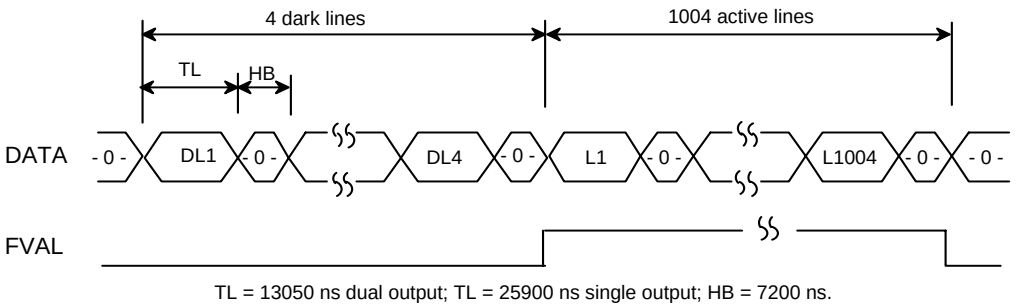


Figure 2.7 - Dual Output Line Timing (IPX-1M48)



TL = 13050 ns dual output; TL = 25900 ns single output; HB = 7200 ns.

Figure 2.8 - Single / Dual Output Frame Timing (IPX-1M48)

IPX-2M30

In the single mode, each line consists of 4 empty pixels (E1 – E4), followed by 16 masked pixels used for black (dark) reference (R1 – R16), followed by 4 buffer pixels (B1 – B4), followed by 1600 active data pixels (D1 – D1600), followed by 4 buffer pixels (B1 – B4), and followed by another 16 masked dark pixels (R1 – R16) – Figure 2.9. In the dual mode, each line consists of 4 empty pixels (E1 – E4), followed by 16 masked pixels used for black (dark) reference (R1 – R16), followed by 4 buffer pixels (B1 – B4), followed by 800 active data pixels – Figure 2.10. The data is sampled on the rising edge of the clock, and the LVAL (line valid) signal is active only during the active pixels. Each frame consists of 82 us vertical frame timing for single mode (62 us for dual mode) followed by 2 masked dark lines RL1, RL2, followed by 4 buffer lines (B1 – B4), followed by 1200 active lines (L1 – L1200), followed by 4 buffer lines (B1 – B4), and followed by another 4 masked dark lines (R1 – R4). During each frame the FVAL (frame valid) signal is active only during the active lines (L1 – L1200) – Figure 2.11.

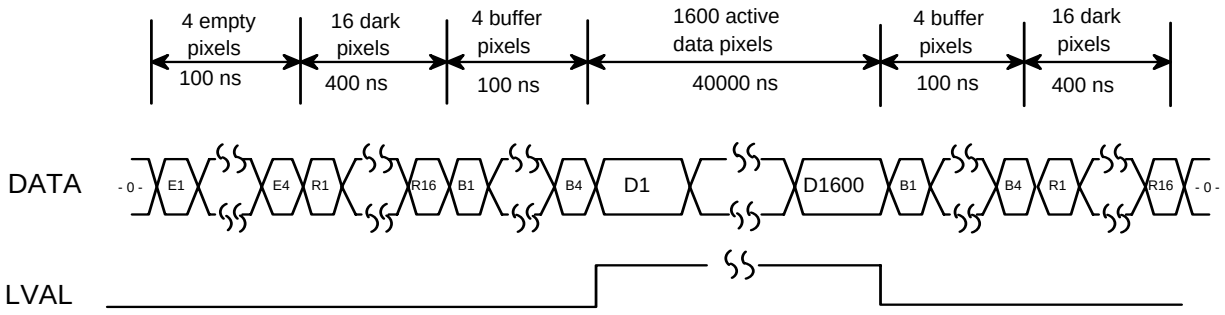


Figure 2.9 - Single output line timing (IPX-2M30)

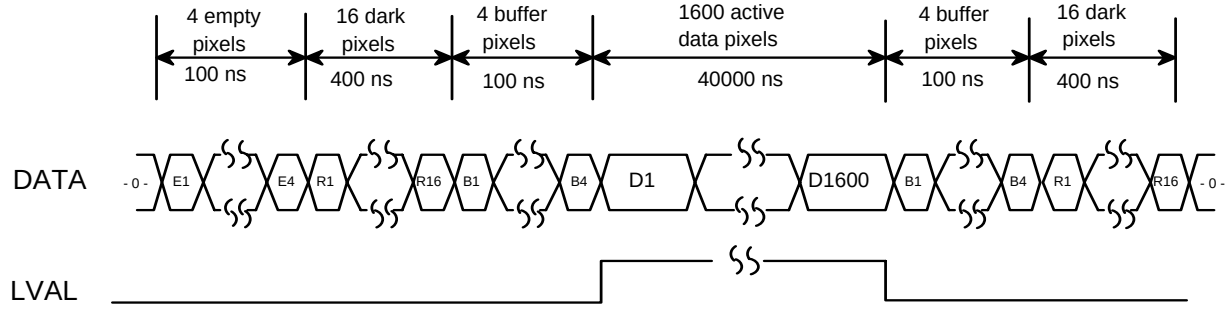
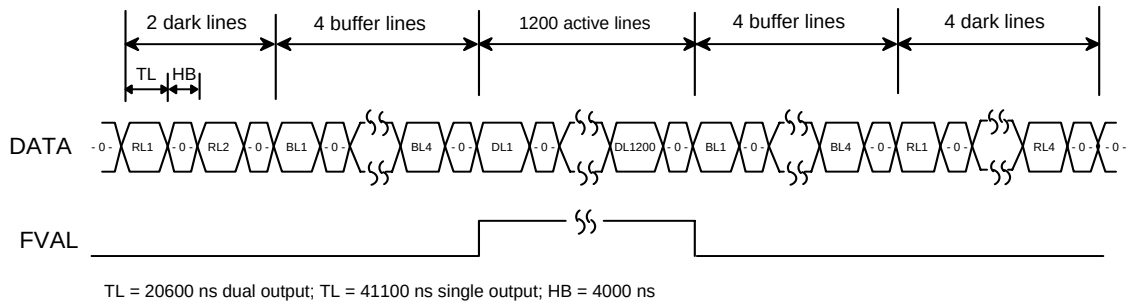


Figure 2.10 - Dual output line timing (IPX-2M30)



TL = 20600 ns dual output; TL = 41100 ns single output; HB = 4000 ns

Figure 2.11 - Single / Dual Output Frame Timing (IPX-2M30)

In the single mode, each line consists of 4 empty pixels (E1 – E4), followed by 28 masked pixels used for black (dark) reference (R1 – R28), followed by 4 buffer pixels (B1 – B4), followed by 1920 active data pixels (D1 – D1920), followed by 4 buffer pixels (B1 – B4), and followed by another 28 masked dark pixels (R1 – R28) – Figure 2.12. In the dual mode, each line consists of 4 empty pixels (E1 – E4), followed by 28 masked pixels used for black (dark) reference (R1 – R28), followed by 4 buffer pixels (B1 – B4), followed by 960 active data pixels (D1 – D960) – Figure 2.13. The data is sampled on the rising edge of the clock, and the LVAL (line valid) signal is active only during the active pixels. Each frame consists of 90.6 us vertical frame timing for single mode (65.9 us for dual mode), followed by 4 masked dark lines (RL1 – RL4), followed by 2 buffer lines (B1, B2), followed by 1080 active lines (L1 – L1080), followed by 2 buffer lines (B1, B2), and followed by another 4 masked dark lines (R1 – R4). During each frame the FVAL (frame valid) signal is active only during the active lines (L1 – L1080) – Figure 2.14.

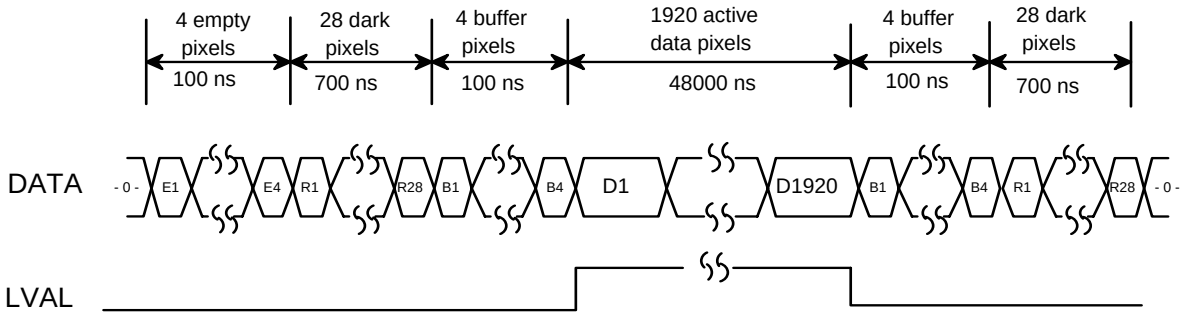


Figure 2.12 - Single Output Line Timing (IPX-2M30H)

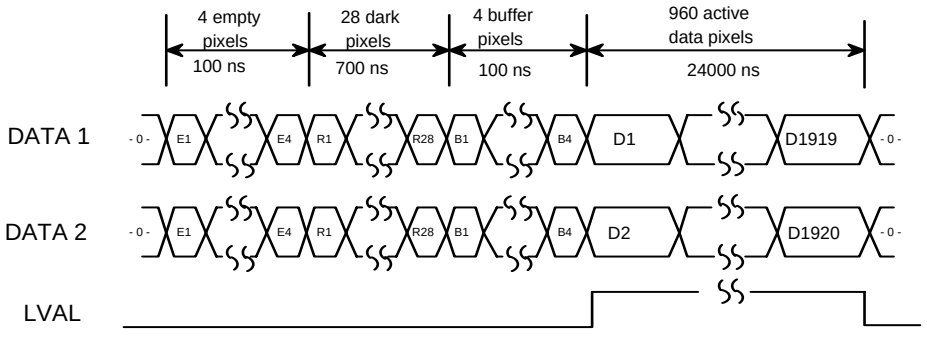


Figure 2.13 - Dual Output Line Timing (IPX-2M30H)

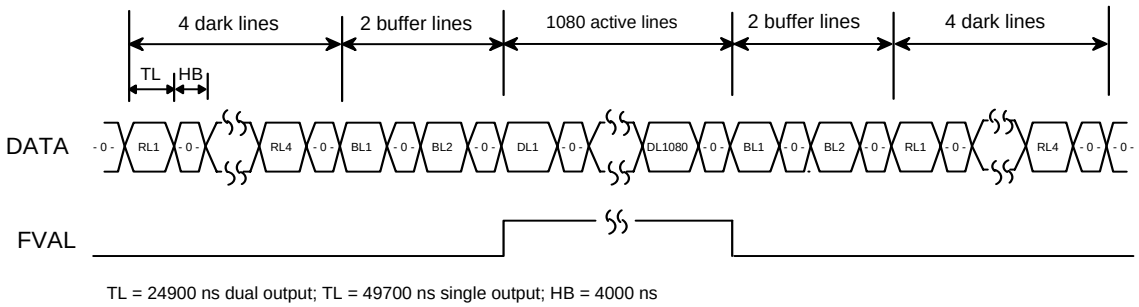


Figure 2.14 - Single / Dual Output Frame Timing (IPX-2M30H)

IPX-4M15

In single mode, each line consists of 12 empty pixels (E1 – E12), followed by 28 masked pixels used for black (dark) reference (R1 – R28), followed by 4 buffer pixels (B1 – B4), followed by 2048 active data pixels (D1 – D2048), followed by 4 buffer pixels (B1 – B4), and followed by another 28 masked dark pixels (R1 – R28) – Figure 2.15. In the dual mode, each line consists of 12 empty pixels (E1 – E12), followed by 28 masked pixels used for black (dark) reference (R1 – R28), followed by 4 buffer pixels (B1 – B4), followed by 1024 active data pixels – Figure 2.16. The data is sampled on the rising edge of the clock, and the LVAL (line valid) signal is active only during the active pixels. Each frame consists of 122.1 us vertical frame timing for single mode (95.7 us for dual mode), followed by 10 masked dark lines RL1 – RL10, followed by 6 buffer lines (B1 – B6), followed by 2048 active lines (L1 – L2048), and followed by 8 buffer lines (B1 – B8). During each frame the FVAL (frame valid) signal is active only during the active lines (L1 – L2048) – Figure 2.17.

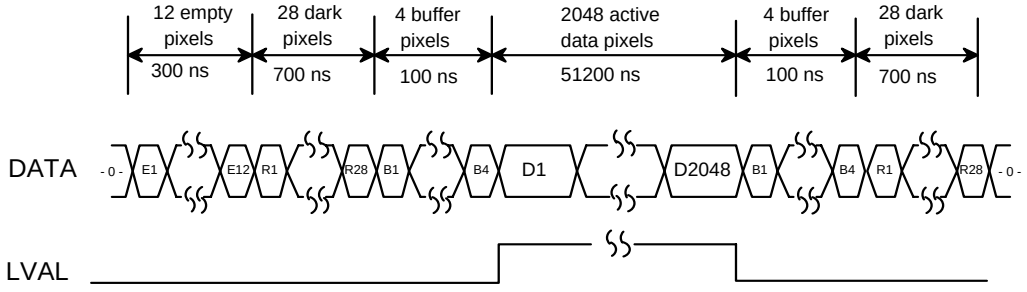


Figure 2.15 - Single Output Line Timing (IPX-4M15)

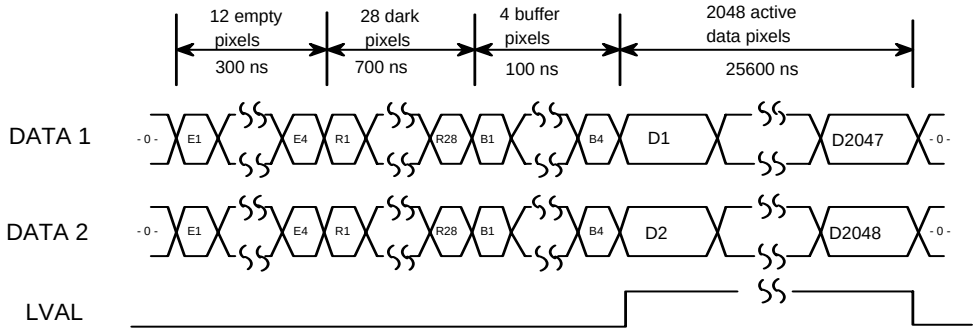
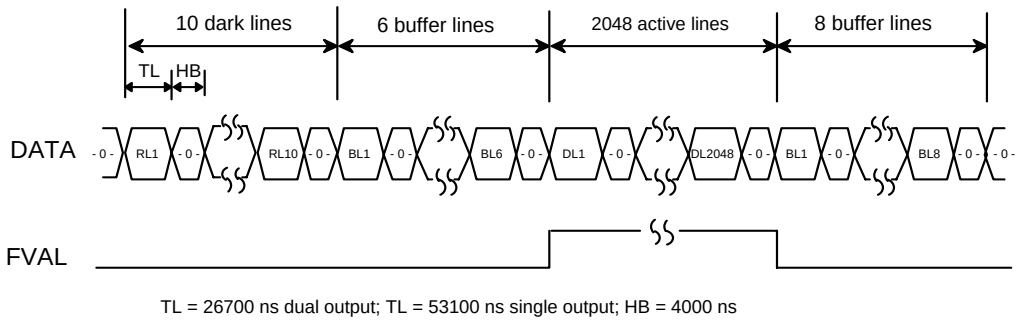


Figure 2.16 - Dual Output Line Timing (IPX-4M15)



TL = 26700 ns dual output; TL = 53100 ns single output; HB = 4000 ns

Figure 2.17 - Single / Dual Output Frame Timing (IPX-4M15)

IPX-11M5

In the single mode, each line consists of 4 empty pixels (E1 – E4), followed by 20 masked pixels used for black reference (R1 – R20), followed by 16 buffer pixels (B1 – B16), followed by 4000 active data pixels (D1 – D4000), followed by 16 buffer pixels (B1 – B16), and followed by another 20 masked dark pixels (R1 – R20) – Figure 2.18 In the dual mode, each line consists of 4 empty pixels (E1 – E4), followed by 20 masked pixels used for black reference (R1 – R20), followed by 16 buffer pixels (B1 – B16), followed by 2000 active data pixels – Figure 2.19. The data is sampled on the rising edge of the clock, and the LVAL (line valid) signal is active only during the active pixels. Each frame consists of 282 us vertical frame timing for single mode (206 us for dual mode), followed by 16 masked dark lines (RL1 – RL16), followed by 8 buffer lines (B1 – B8), followed by 2672 active lines (L1 – L2672), and followed by 8 buffer lines (B1 – B8), and followed by 16 masked dark lines (RL1 – RL16). During each frame the FVAL signal is active only during the active lines (L1 – L2672) – Figure 2.20.

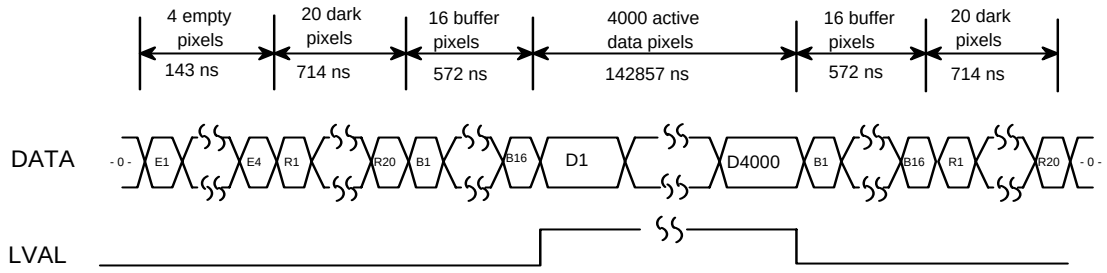


Figure 2.18 - Single Output Line Timing (IPX-11M5)

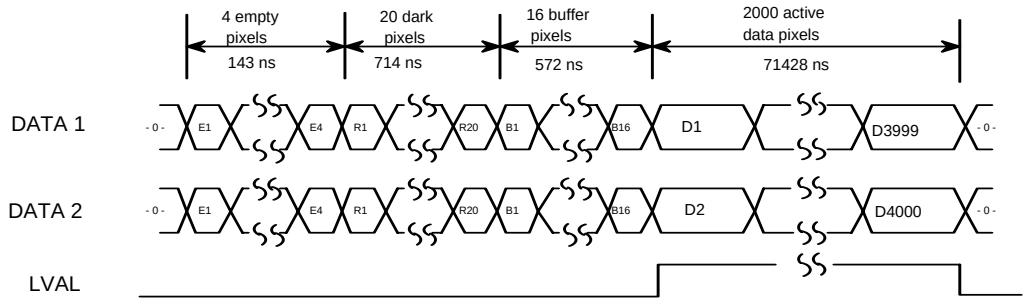
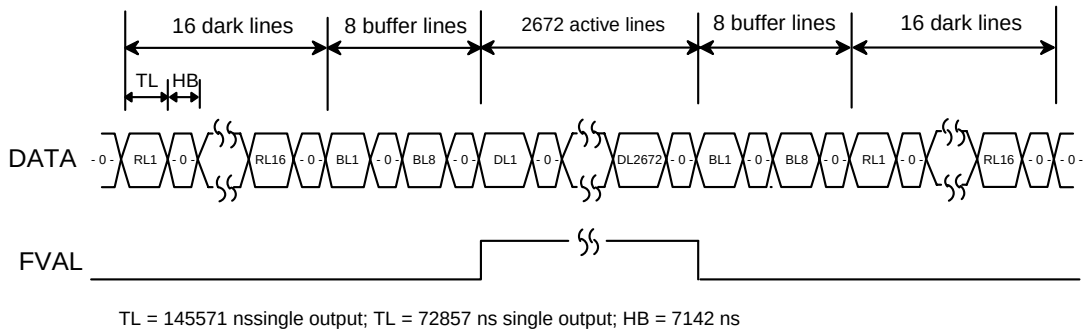


Figure 2.19 - Dual Output Line Timing (IPX-11M5)



TL = 145571 nssingle output; TL = 72857 ns single output; HB = 7142 ns

Figure 2.20 - Single / Dual Output Frame Timing (IPX-11M5)

2.2 AREA OF INTEREST

2.2.1 Horizontal and Vertical Window

Horizontal and vertical windowing (Area Of Interest) is supported in all IPX cameras. Emphasizing a particular area of interest in horizontal direction is possible by using a horizontal window feature, where the beginning part of each line (pixel 1 to 'Start Pixel') and the end of each line ('End Pixel' to Last pixel) are ignored – Figure 2.9. The precision of each pointer (beginning and end of the window) is 1 pixel, and can be placed in the entire image area (in dual mode the horizontal AOI is symmetrical around the image center) – refer to the camera configuration section. The minimum window size is one pixel for single mode (or 2 pixels for dual mode), and the maximum window size is the full resolution (Last H pixel). Table 2.2 shows the allowable values for the 'Start Pixel' and the 'End Pixel'.

Emphasizing a particular area of interest in vertical direction is possible by using a vertical window feature. Vertical windowing is used for increasing the frame rates. For example, by skipping half of the lines, the image will be sub-windowed by a factor of 2 and the frame rate will almost double. The vertical window beginning (Start Line) and (End Line) can be programmed with a precision of one line – Figure 2.21. The minimum window size is one line, the maximum is full vertical resolution (Last V line). Table 2.2 shows the allowable values for the 'Start Line' and the 'End Line'.

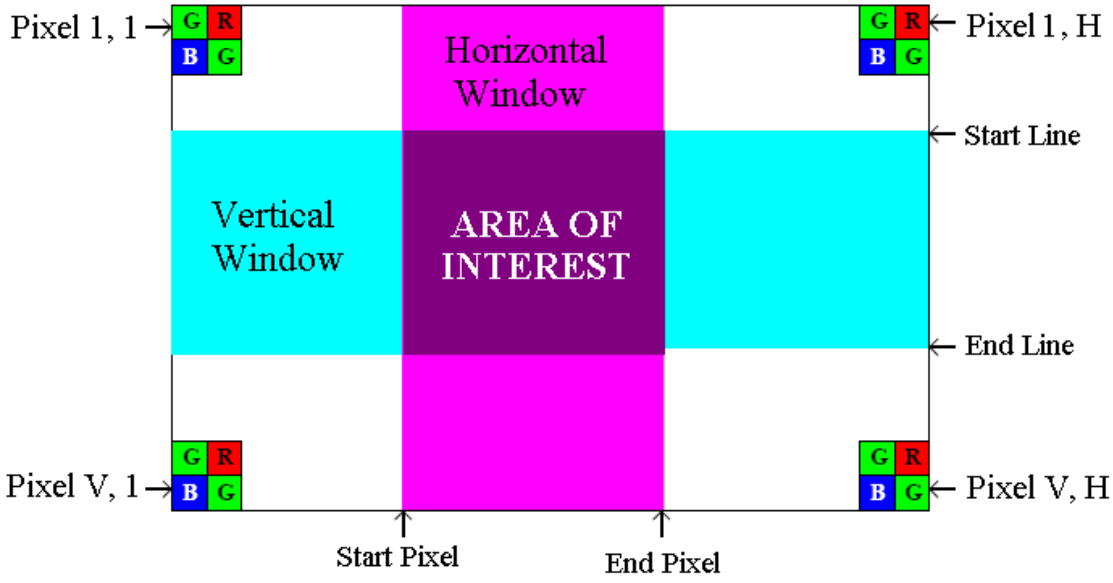


Figure 2.21 - Horizontal and Vertical Window Positioning

Feature	IPX-VGA	IPX-1M48	IPX-2M30	IPX-2M30H	IPX-4M15	IPX-11M5
Start Pixel - Min.	1	1	1	1	1	1
Start Pixel - Max.	639	1003	1599	1919	2047	3999
End Pixel - Min.	2	2	2	2	2	2
End Pixel - Max.	640	1004	1600	1920	2048	4000
Last H Pixel	640	1004	1600	1920	2048	4000
Start Line - Min.	1	1	1	N/A	1	1
Start Line - Max.	479	1003	1199	N/A	2047	2671
End Line - Min.	2	2	2	N/A	2	2
End Line - Max.	480	1004	1200	N/A	2048	2672
Last V Line	480	1004	1200	1080	2048	2672

Table 2.2 - Allowable Horizontal and Window Sizes

CAUTION NOTE

1. Horizontal and vertical windows can be enabled in all camera modes.
2. The size of the horizontal window does not affect the frame rate.
3. The frame-grabber horizontal and vertical resolutions must be adjusted for each window size.
   a. The horizontal resolution is equal to the window size, which is: 'End Pixel' - 'Start Pixel' + 1.
   b. The vertical resolution is equal to the window size which is: 'End Line' - 'Start Line' + 1
4. Positioning the horizontal window outside the image window will result in an error.
5. Color version users – for proper color reconstruction 'Start pixel' and 'Start Line' must be an odd number.
6. Vertical window feature is not available in IPX-2M30H

2.2.2 Calculating the Frame Rate Using Vertical Window

The resulting frame rate (FR) for each camera can be approximately calculated using formulas 2.1a – 2.1f, where WS is the window size. The window size is the number of lines in the window (WS = 'End Line' – 'Start Line' + 1). Figure 2.22 – 2.27 show a graphical representation of the formulas.

IPX-VGA120

FR [fps] = 1 / [(0.70 x 10^{-6} x (492 – WS)) + T_{VT} + (WS x T_L)] (2.1a)

T_{VT} is a constant = 35.35 x 10^{-6} (for IPX-VGA120), and T_L is the active line duration (T_L = 18.38 x 10^{-6} for IPX-VGA120).

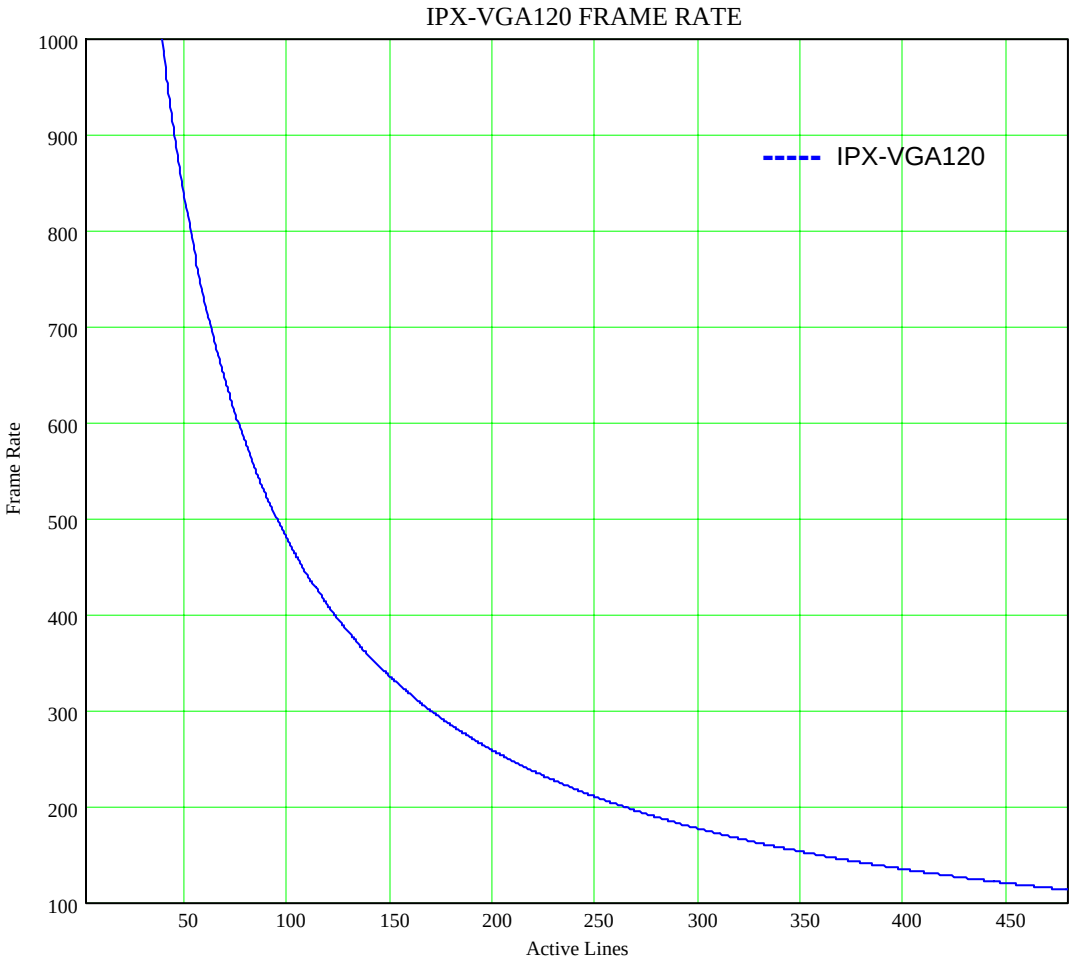


Figure 2.22 - Frame Rate vs. Vertical Window Size (IPX-VGA120)

IPX-VGA210

FR [fps] = 1 / [(0.70 x 10^{-6} x (492 – WS)) + T_{VT} + (WS x T_L)] (2.1b)

T_{VT} is a constant (T_{VT} = 35.35 x 10^{-6} for single and dual mode), and T_L is the active line duration (T_L = 18.38 x 10^{-6} for single mode, T_L = 9.7 x 10^{-6} for dual mode).

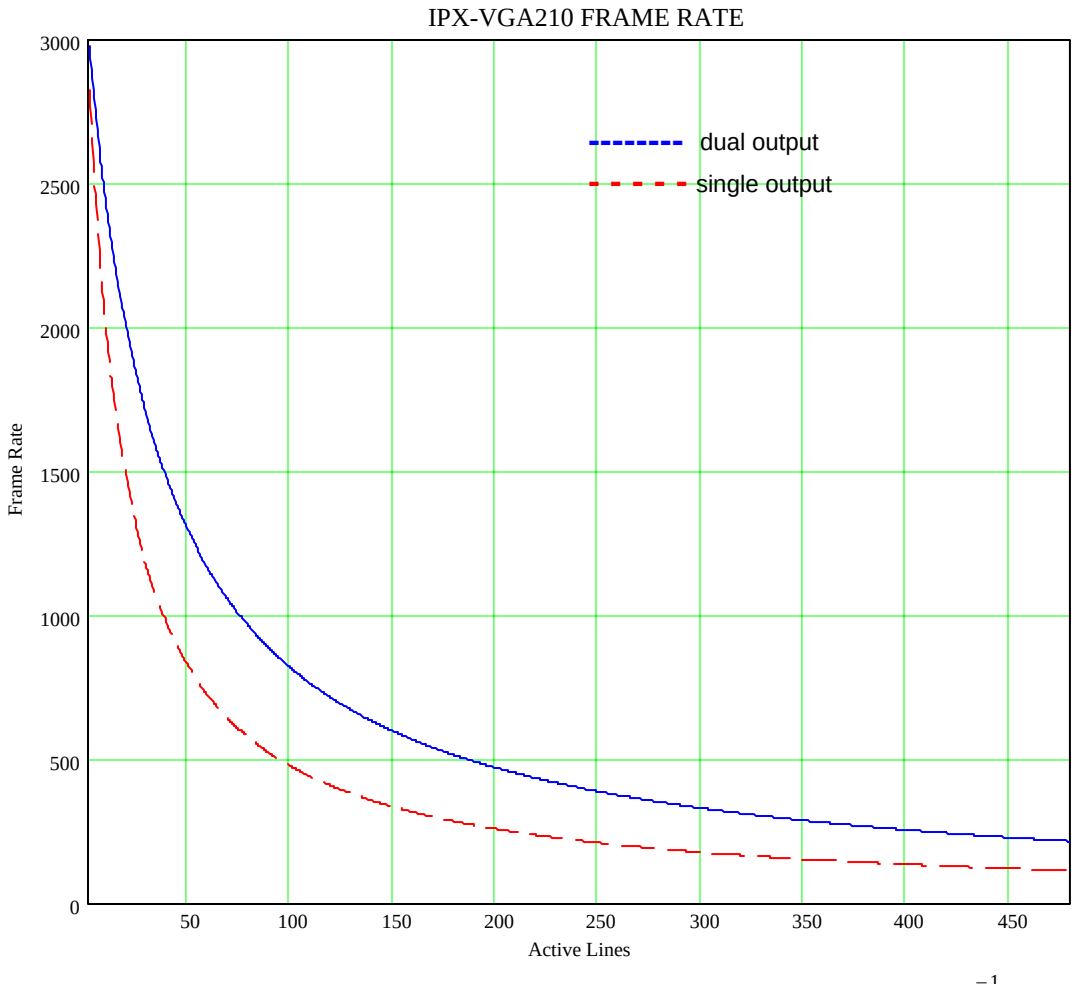


Figure 2.23 - Frame Rate vs. Vertical Window Size (IPX-VGA210)

IPX-1M48

FR [fps] = 1 / [(7.2 x 10^{-6} x (1010 – WS)) + T_{VT} + (WS x T_L)] (2.1c)

T_{VT} is a constant (T_{VT} = 60.90 x 10^{-6} for single and dual mode), and T_L is the active line duration (T_L = 33.1 x 10^{-6} for single mode, and T_L = 20.3 x 10^{-6} for dual mode).

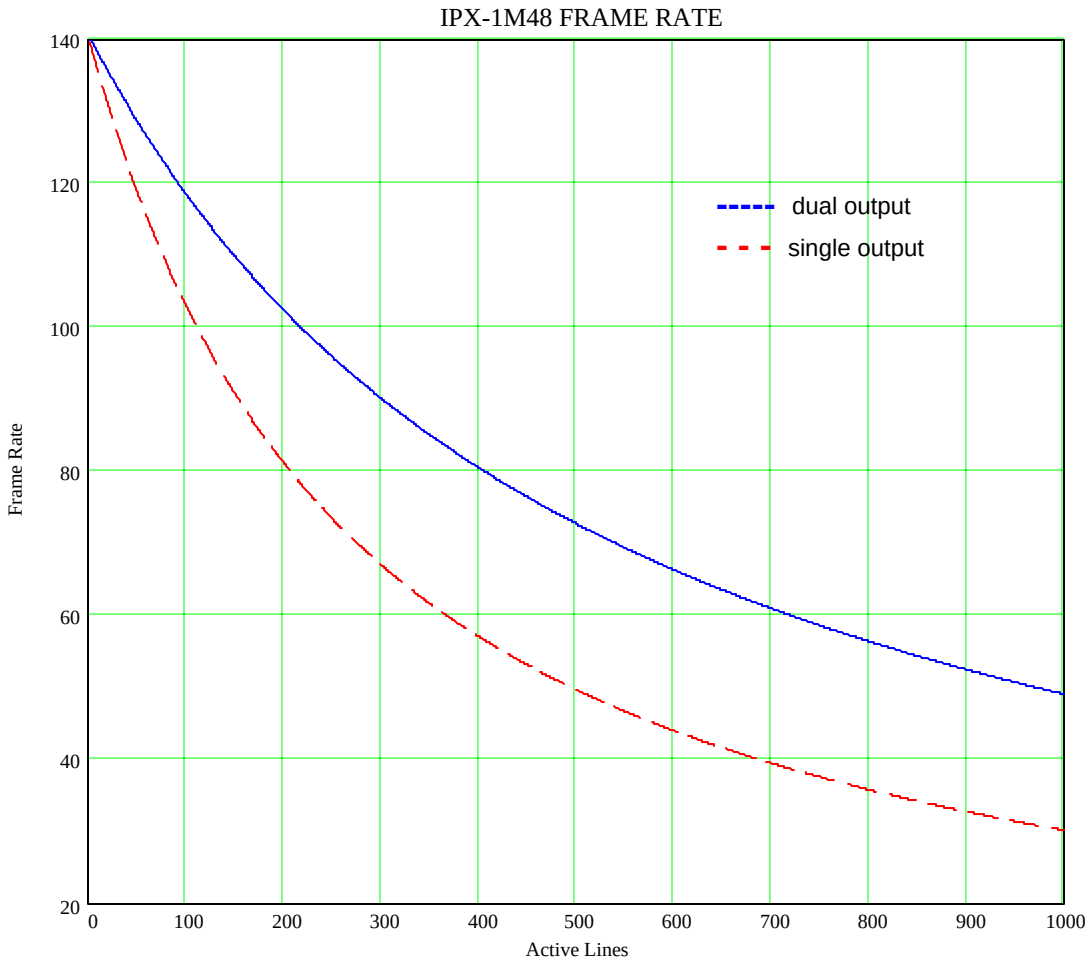


Figure 2.24 - Frame Rate vs. Vertical Window Size (IPX-1M48)

IPX-2M30

FR [fps] = 1 / [(4.00 x 10^{-6} x (1214 – WS)) + T_{VT} + (WS x T_L)] (2.1d)

T_{VT} is a constant (T_{VT} = 82 x 10^{-6} for single mode, and T_{VT} = 62 x 10^{-6} for dual mode), and T_L is the active line duration (T_L = 45.18 x 10^{-6} for single mode, and T_L = 24.7 x 10^{-6} for dual mode).

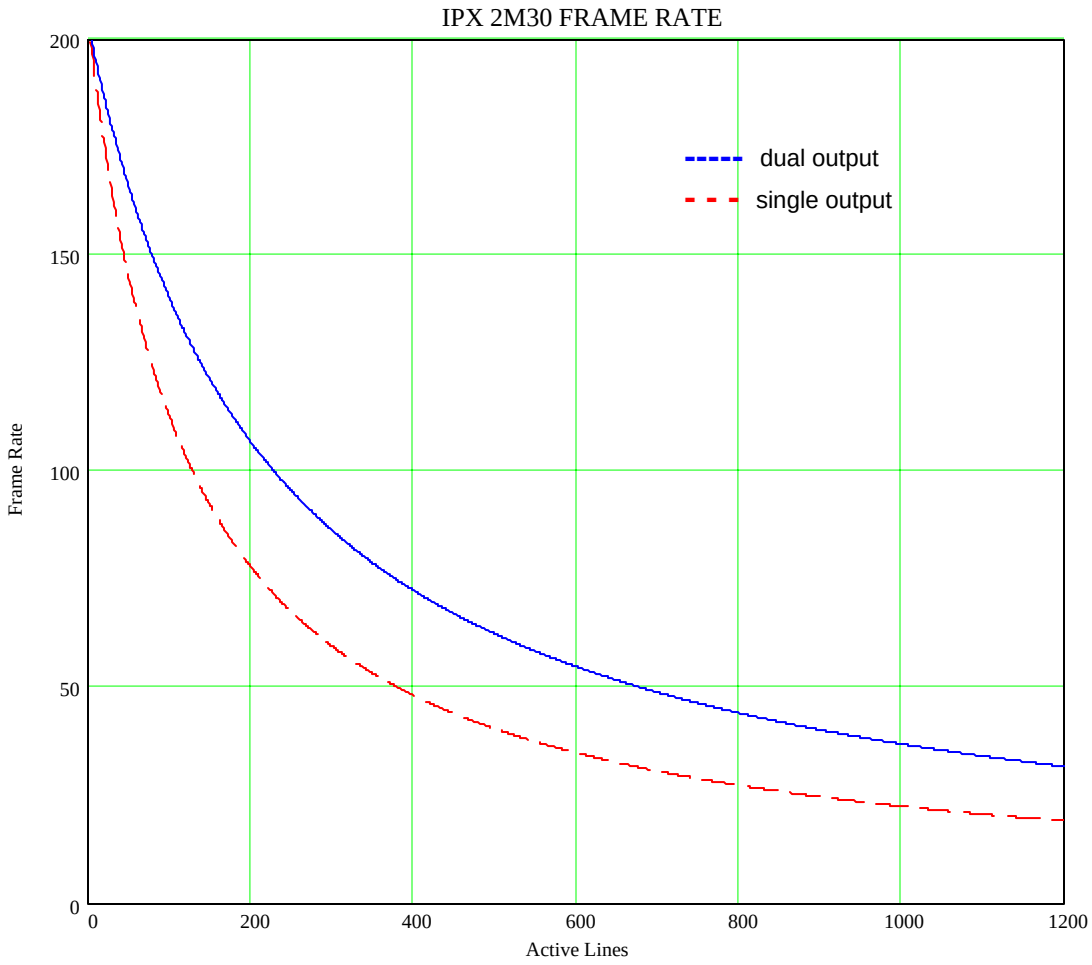


Figure 2.25 - Frame Rate vs.Vertical Window Size (IPX-2M30)

IPX-4M15

$$FR\ [fps] = 1 / [(4.00 \times 10^{-6} \times (2072 - WS)) + T_{VT} + (WS \times T_L)] \quad (2.1e)$$

T_{VT} is a constant ($T_{VT} = 122.1 \times 10^{-6}$ for single mode, and $T_{VT} = 95.7 \times 10^{-6}$ for dual mode), and T_L is the active line duration ($T_L = 57.38 \times 10^{-3}$ for single mode, and $T_L = 30.8 \times 10^{-3}$ for dual mode).

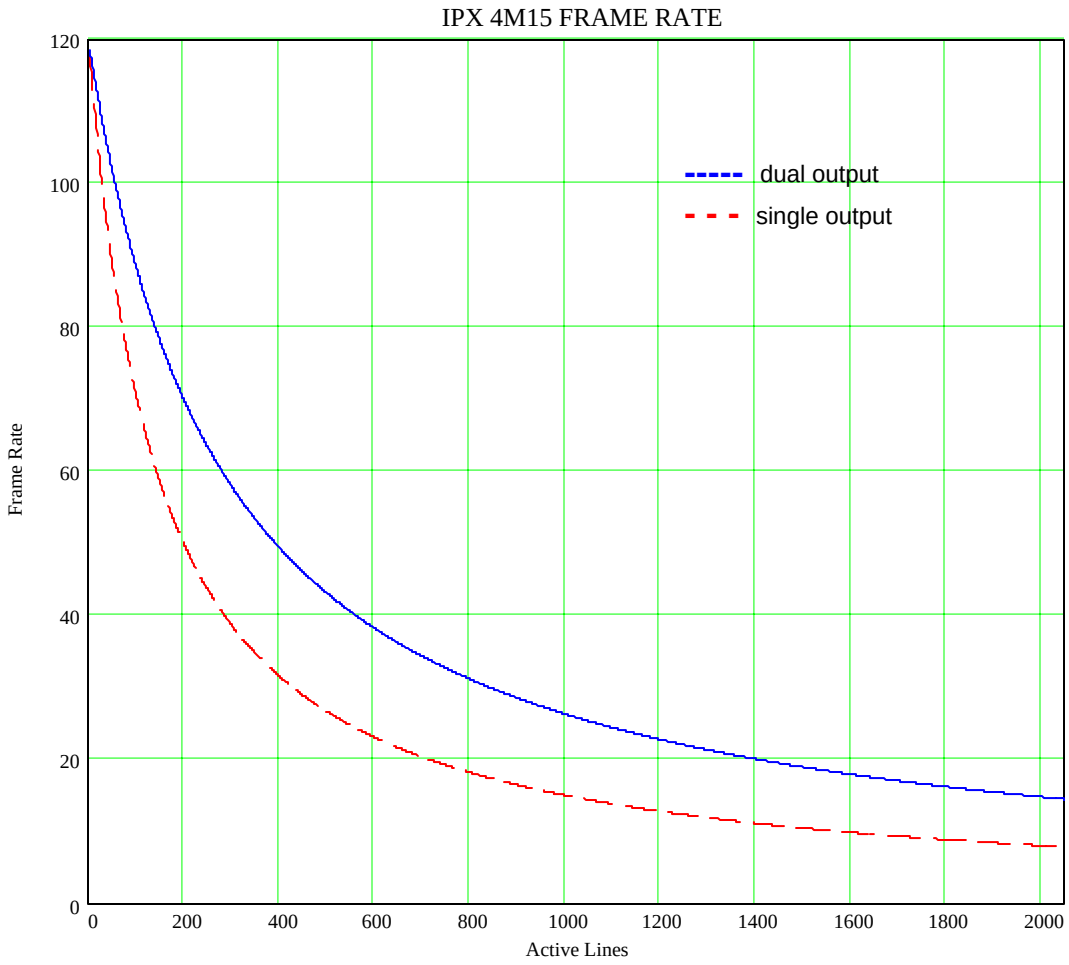


Figure 2.26 - Frame Rate vs. Vertical Window Size (IPX-4M15)

IPX-11M5

$$FR\ [fps] = 1 / [(10.50 \times 10^{-6} \times (2720 - WS)) + T_{VT} + (WS \times T_L)] \quad (2.1f)$$

T_{VT} is a constant ($T_{VT} = 282.14 \times 10^{-6}$ for single mode, and $T_{VT} = 206.07 \times 10^{-6}$ for dual mode), and T_L is the active line duration ($T_L = 152.82 \times 10^{-6}$ for single mode, and $T_L = 80.14 \times 10^{-6}$ for dual mode).

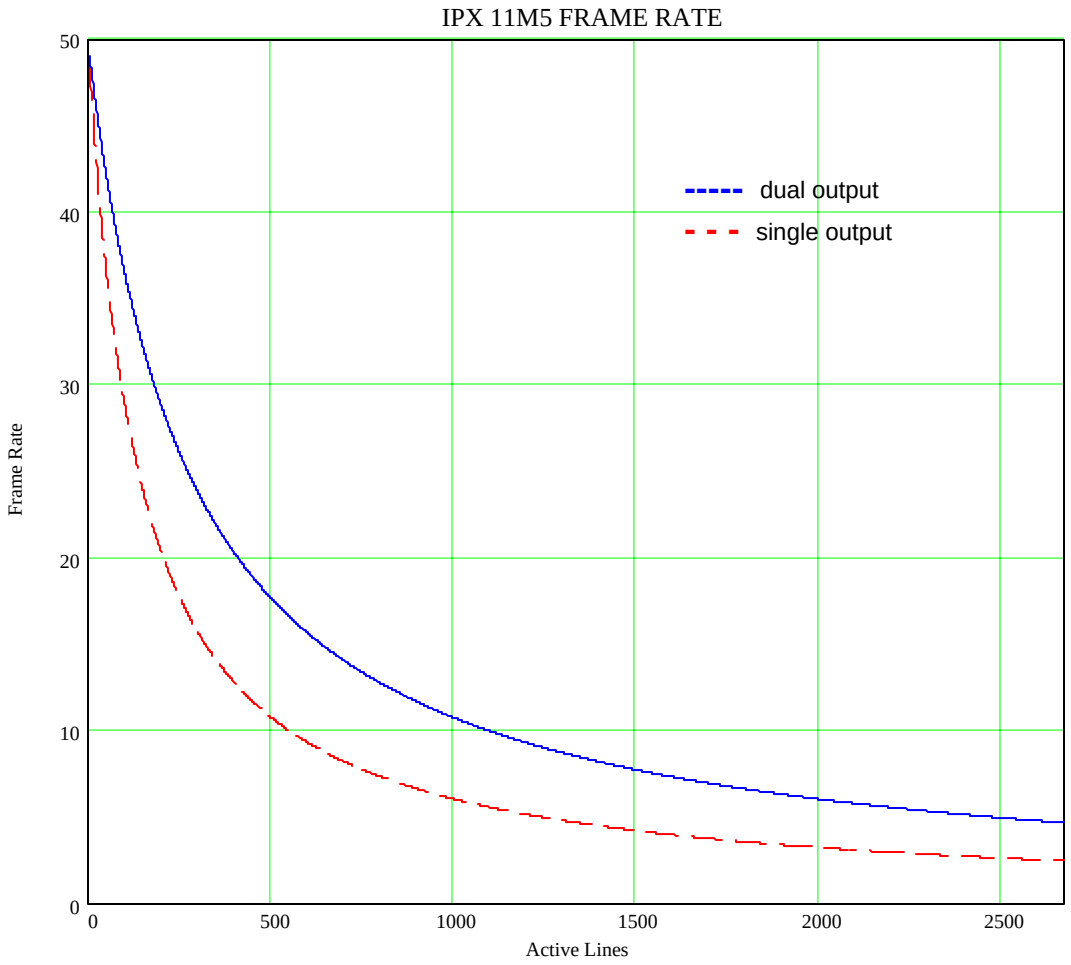


Figure 2.27 - Frame Rate vs. Vertical Window Size (IPX-11M5)

2.3 BINNING

Binning uses the CCD sensor to combine adjacent pixels in both directions to effectively create larger pixels and less resolution. In 2:1 horizontal binning mode, two adjacent pixels in each line are summed together (in the horizontal direction), For example, pixels 1+2, 3+4, 5+6, … in each line are summed together. Horizontal binning does not affect the frame rate. It does, however, reduce the horizontal resolution by a factor of 2. This occurs because when binning two pixels together, only half of the pixels per line remain. Horizontal binning is equivalent to 2:1 sub-sampling in the horizontal direction. In horizontal binning mode, the entire image is captured and displayed, which is different than horizontal windowing, where only a portion of the image is captured and displayed.

Vertical binning 2:1 is a readout mode of progressive scan CCD image sensors where two image lines are clocked simultaneously into the horizontal CCD register before being read out. This results in summing the charges of adjacent pixels (in the vertical direction) from two lines. For example, the corresponding pixels in lines 1+2, 3+4, 5+6, … are summed together. Vertical binning reduces the vertical resolution by a factor of 2, and almost doubles the frame rate. This occurs because when binning two lines together, only half of the lines need to be read out. Vertical binning is equivalent to 2:1 sub-sampling in the vertical direction. In vertical binning the entire image is captured and displayed, which is different than vertical windowing, where only a portion of the image is captured and displayed. If horizontal and vertical binning are used simultaneously the image is sub-sampled by 4 and the aspect ratio is preserved.

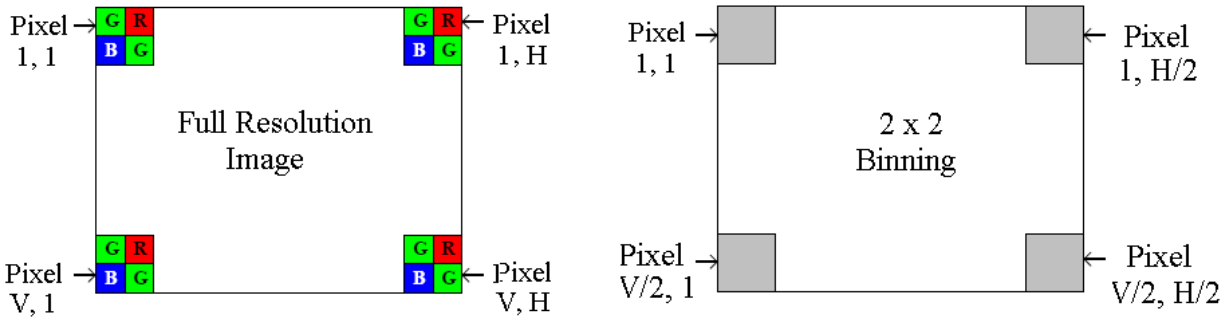


Figure 2.28 - Horizontal and Vertical Binning

CAUTION NOTE

1. Horizontal or vertical binning used alone changes the aspect ratio of the image in the vertical or horizontal direction. To correct this, use horizontal and vertical binning simultaneously.
2. The frame-grabber vertical and horizontal resolution should be changed to reflect the actual number of active pixels and lines.
3. Vertical binning in single output mode of operation may cause blooming for saturated signal levels.
4. Color version users – horizontal or vertical binning used alone will create color distortions. If used simultaneously, the resulting image will be monochrome.

2.4 EXPOSURE CONTROL

2.4.1 Electronic Shutter

During normal camera operation, the exposure time is fixed and determined by the frame rate. The electronic shutter can be used to precisely control the image exposure time under bright light conditions. The electronic shutter does not affect the frame rate, it only reduces the amount of electrons collected. The desired exposure time is set by positioning a short pulse, SHUTTER, with respect to the vertical transfer pulse, VCCD – Figure 2.29. The electronic shutter pulse can be positioned within the entire frame timing period with a precision of 1 line (4 lines for IPX-1M48).

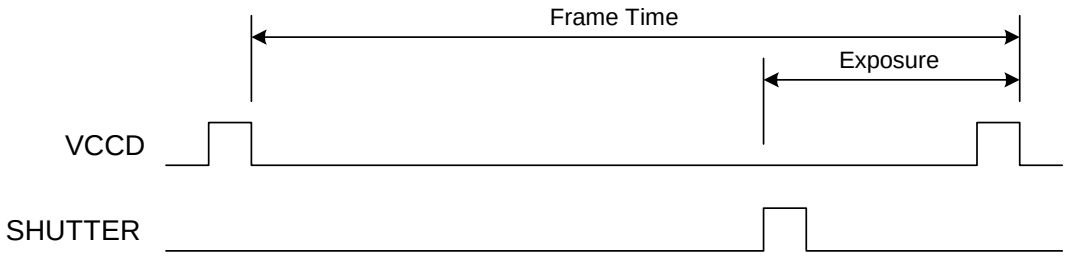


Figure 2.29 - Electronic Shutter Position

CAUTION NOTE

1. The electronic shutter can be enabled in all camera modes.
2. Positioning the shutter signal outside the frame window will result in an error.

2.4.2 Long Integration

Long integration is used for extending the image exposure time beyond the standard frame time. During normal camera operation, the minimum frame rate determines the maximum exposure time. The desired exposure time can be adjusted (increased) by moving the vertical transfer pulse, VCCD, beyond the normal exposure range – Figure 2.30. The integration time can be programmed in 10 millisecond increments from 10 ms (camera dependent) up to 10 seconds. Enabling long integration reduces the frame rate. The resultant frame rate can be calculated using formula 4.2. This mode is displayed on the LED by slow pulsation with a 2 second interval – refer to Status LED section.

Frame rate [fps] = 1 / long integration time [sec] (4.2)

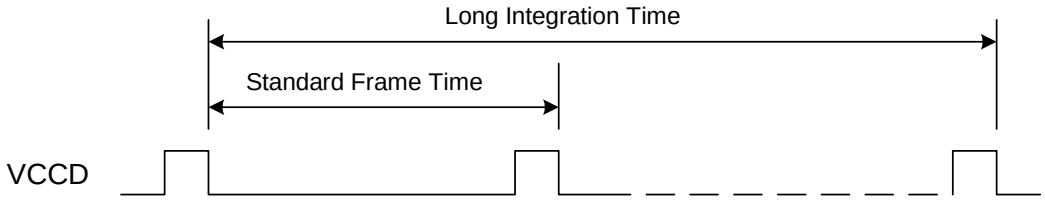


Figure 2.30 - Long Integration

CAUTION NOTE

1. During the integration time the camera has to be kept still otherwise a motion smear will appear on the image.
2. The minimum value for long integration is camera dependent:
   - IPX-VGA210/210 – 10 ms.
   - IPX-1M48 – 30 ms.
   - IPX-2M30/H – 70 ms.
   - IPX-4M15 – 120 ms.
   - IPX-11M5 – 420 ms.
3. Long Integration cannot be enabled in Trigger mode.
4. Long Integration cannot be enabled in Programmable Frame Rate mode.
5. Long Integration cannot be enabled in Shutter mode.
6. Long time integration significantly decreases the signal to noise ratio. More electrons will be collected from the pixels dark current and thus the camera noise will increase significantly.

2.5 EXTERNAL TRIGGER

In the normal mode of operation, the camera is free running. Using the external trigger mode allows the camera to be synchronized to an external timing pulse. There are two general modes available for external triggering – software and hardware.

In hardware triggering mode the camera receives the trigger signal coming from the connector located on the back of the camera. The hardware trigger input is optically isolated from the rest of the camera hardware - Figure 2.31. The input signals "+ TRIGGER IN" and "– TRIGGER IN" are used to connect to an external trigger source. On the edge of the external pulse which creates a positive voltage difference between "+ TRIGGER IN" and "– TRIGGER IN", a trigger signal is sent to the camera. The voltage difference between the trigger inputs "+ TRIGGER IN" and "– TRIGGER IN" must be positive between 3.3 and 5.0 volts. To limit the input current a 300 ohm internal resistor is used, but the total maximum current MUST NOT exceed 25 mA. The actual trigger pulse duration does not affect the integration time. The integration time for the first frame is determined by the Pre-Exposure register. The minimum duration of the trigger pulse is 100 microseconds. There are no restrictions for the maximum pulse duration, but it is recommended that the trigger pulse is kept as short as possible, especially if a series of pulses are used.

In software triggering mode the camera receives the trigger signal coming from the frame grabber via camera control signal CC1. In this mode the integration time for the first frame is determined by the duration of the actual CC1 trigger pulse.

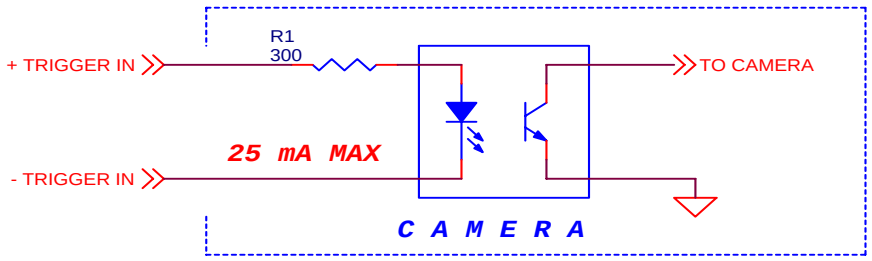


Figure 2.31 - Hardware Trigger Electrical Connection

2.5.1 Standard Triggering - Programmable Exposure

When the standard triggering mode is enabled, the camera idles and waits for a trigger signal. Upon receiving the external trigger signal, the camera clears the horizontal and vertical registers, sends one 5 microseconds shutter pulse to clear the pixels and starts integration. The exposure time for the

first frame can be programmed. For IPX-VGA - from 500 usec to 32 msec (in 500 microseconds increments). For IPX-1M48, IPX-2M30 and IPX-2M30H - from 1 msec to 64 msec (in 1.0 msec increments). For IPX-4M15 - from 2 msec to 128 msec (in 2 msec increments). For IPX-11M5 - from 5 msec to 320 msec (in 5 msec increments). There is a fixed additional delay of 10 usec (because of the shutter pulse) between the rising edge of the trigger pulse and the beginning of the integration – Figure 2.32. If the CC1 input is used - the duration of the CC1 trigger pulse is used to determine the first frame exposure time. After the first frame has been exposed, the camera is free running, where the frame rate determines the exposure time. The number of frames captured after the trigger pulse goes high can be programmed from 1 to 250 frames, or to be free-running – refer to the 'std' command. Along with the shutter pulse, the camera sends one strobe pulse (200 microseconds duration) for synchronization with an external strobe. This pulse is always present in the external trigger mode.

CAUTION NOTE

1. Enabling several trigger options at the same time will result in an error – refer to Status LED section.
2. For proper operation - if series of trigger pulses are used, make sure that the timing interval between them is greater than the corresponding frame duration – refer to section 2.1.4 Timing Diagrams.

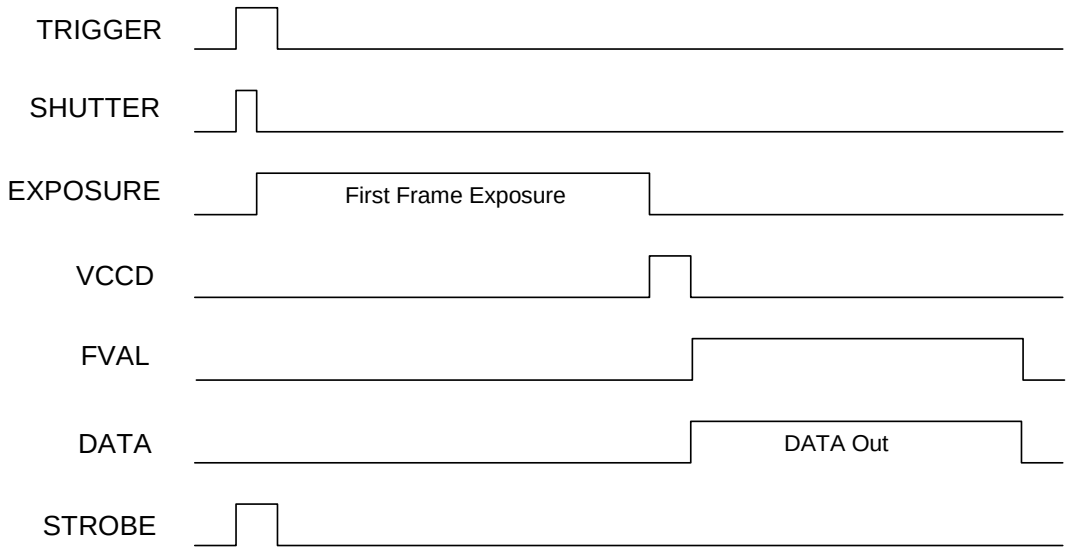


Figure 2.32 - Standard Triggering Timing

2.6 STROBE OUTPUT

2.6.1 Strobe Positioning

The strobe output is used to synchronize an external light source with the camera timing, and thus to maximize the camera efficiency in low light level conditions. The optimal strobe signal position is achieved by the positioning of a short pulse, STROBE, (duration 200 µs) with respect to the vertical transfer pulse VCCD - Figure 2.33. The strobe pulse can be positioned within the entire frame period with a precision 1 line (4 lines for IPX-1M48).

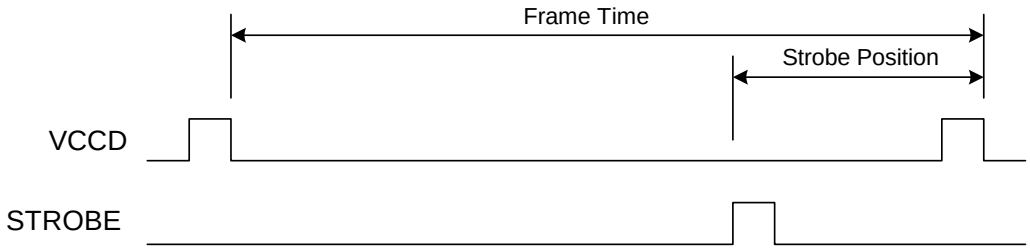


Figure 2.33 - Strobe Pulse Positioning

CAUTION NOTE

1. The strobe output can be enabled in all camera modes.
2. Positioning the strobe signal outside the frame window will result in error – refer to Status LED section.

2.6.2 Strobe Electrical Connectivity

The strobe output is optically isolated from the rest of the camera hardware. To increase the output current to about 40 mA, the output is buffered with a discrete transistor 2N3904 - Figure 2.34. The output signals "+ STROBE" and "– STROBE" are used to connect to an external strobe device. The actual connection depends on the particular implementation. Figure 2.35 shows a sample wiring diagram, which generates a 5 V strobe pulse between "+ STROBE" and "– STROBE". The first one (left) generates an active LOW strobe pulse, and the second one (right) generates an active HIGH strobe pulse.

CAUTION NOTE

1. The maximum voltage difference between the strobe outputs is 8 volts!
2. The maximum output current must not exceed 40mA!

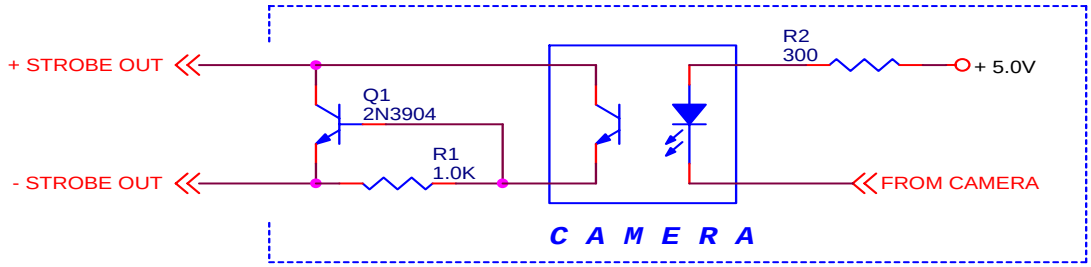


Figure 2.34 - Strobe Output Electrical Connection (Internal)

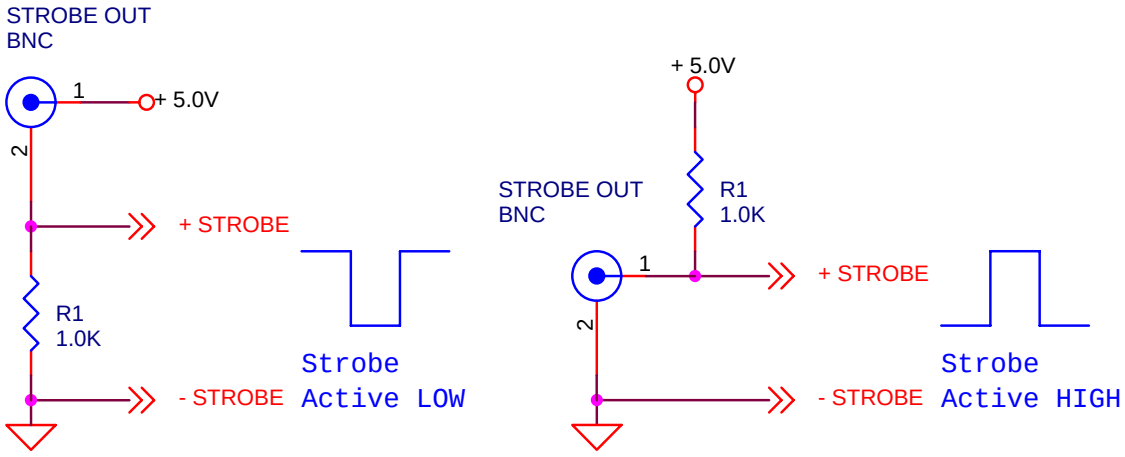


Figure 2.35 – Recommended External Strobe Output Electrical Connection

2.7 GAIN and OFFSET

The camera has dual analog signal processors (or Analog Front End – AFE), one per channel. It features two independent 12 bit 40 MHz processors, each containing a differential input sample-and-hold amplifier (SHA), digitally controlled variable gain amplifier (VGA), black level clamp and a 12-bit ADC. The programmable internal AFE registers include independent gain and black level adjustment. There are 1024 possible gain levels (**gcode** 0 to 1023) and 256 offset (clamp) levels (**ocode** 0 to 255). Figure 2.44 shows the relationship between the video signal output level and gain/offset. Theoretically, the black level should reside at 0 volts and the gain changes should only lead to increasing the amplitude of the video signal. Since the camera has two separate video outputs coming out of the CCD, there is always some offset misbalance between the video outputs. Thus, changing the AFE gain leads to a change in the offset level and to a further misbalance between the two video signals. To correct the balance between two signals for a particular gain, the user should always adjust the offset for each output – refer to the Camera Configuration section. The overall camera gain can be calculated using formula 7.1

$$\text{VGA Gain [dB]} = \text{FG [dB]} + 0.0351 \times \mathbf{gcode} \qquad (7.1)$$

CAUTION NOTE

1. Increasing the gain simultaneously increases the camera noise.
2. Fixed gain (FG) = 0 dB for IPX-1M48, FG = 6dB for the rest of the cameras.

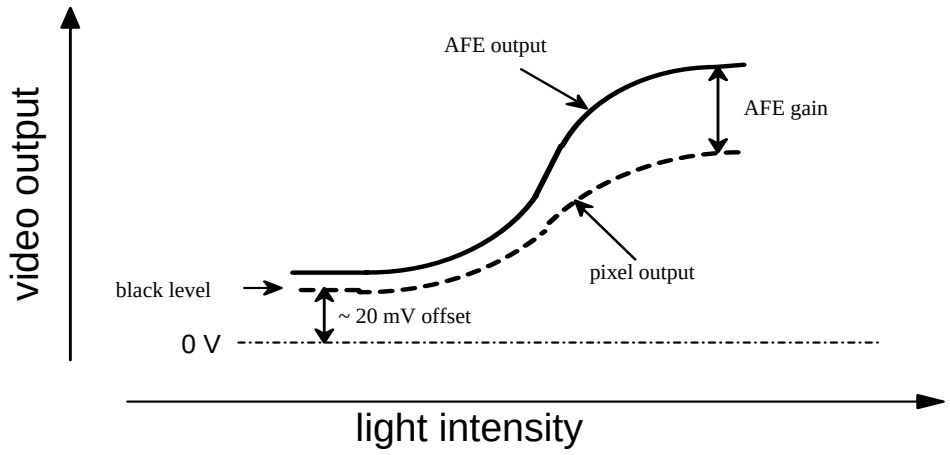


Figure 2.36 - AFE Gain and Offset

2.8 DATA OUTPUT FORMAT

The internal camera processing of the CCD data is performed in 12 bits. The camera can output the data in 12, 10 or 8 bit format. During this standard bit reduction process, the least significant bits are truncated – Figure 2.37.

12 bit output: If the 12 bit original camera data is D0 (LSB) to D11 (MSB), and camera is set to output 12 bit data, the 12 output bits are mapped to D0 (LSB) to D11 (MSB).

10 bit output: If the 12 bit original camera data is D0 (LSB) to D11 (MSB), and camera is set to output 10 bit data, the 10 output bits are mapped to D2 (LSB) to D11 (MSB).

8 bit output: If the 12 bit original camera data is D0 (LSB) to D11 (MSB), and camera is set to output 8 bit data, the 8 output bits are mapped to D4 (LSB) to D11 (MSB).

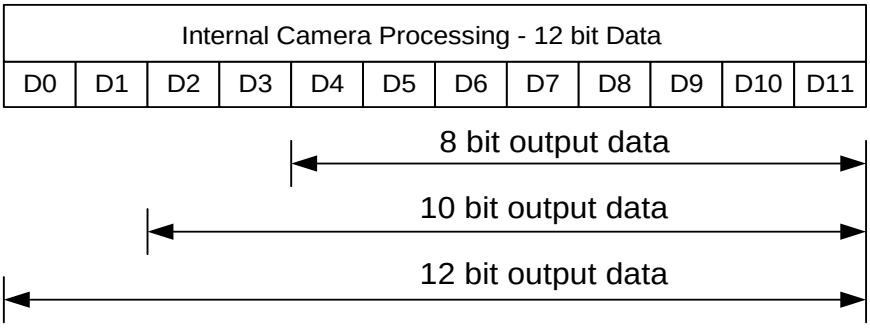


Figure 2.37 - Data Output Format

2.9 GAMMA CORRECTION

The image generated by the camera is normally viewed on a CRT (or LCD) display, which does not have a linear transfer function – i.e., the display brightness is not linearly proportional to the scene brightness (as captured by the camera). As the object brightness is lowered, the brightness of the display correspondingly lowers. At a certain brightness level, the scene brightness decrease does not lead to a corresponding display brightness decrease. The same is valid if the brightness is increased. This is because the display has a nonlinear transfer function and a brightness dynamic range much lower than the camera. The camera has a built-in transfer function to compensate for this non-linearity, which is called gamma correction. If enabled, the video signal is transformed by a non-linear function close to the square root function (0.45 power) – formula 9.1. In the digital domain this is a nonlinear conversion from 12-bit to 10-bit – Figure 2.38. If the camera resolution is set to 10-bit the output resolution after gamma is 8-bit.

$$\text{Output signal [V]} = (\text{input signal [V]})^{0.45} \qquad (9.1)$$

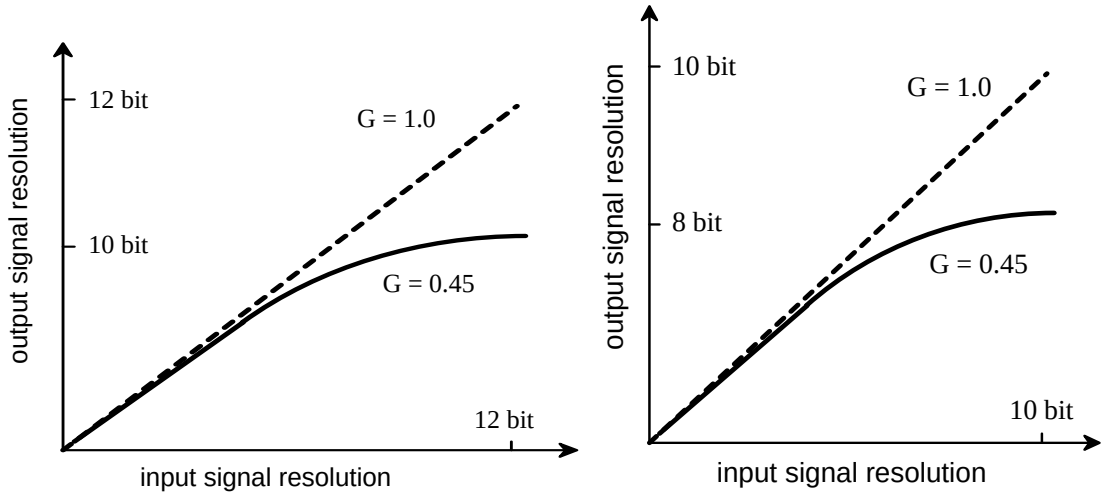


Figure 2.38 - Gamma Corrected Video Signal (12 bit – left, 10 bit – right)

CAUTION NOTE

1. If this mode is enabled 12-bit the user should switch the frame grabber resolution from 12 to 10 bits.
2. If this mode is enabled 10-bit the user should switch the frame grabber resolution from 10 to 8 bits.

2.10 IMAGE REVERSAL

When operating in the image reversal mode, all pixels are shifted to the output in the reverse order. The resultant image appears left/right mirrored in the horizontal direction – Figure 2.39. This feature could be useful if the camera receives a mirrored image (i.e. image coming from a mirror). In this mode the image has a normal vertical orientation and full resolution. This feature is available only in single output mode.

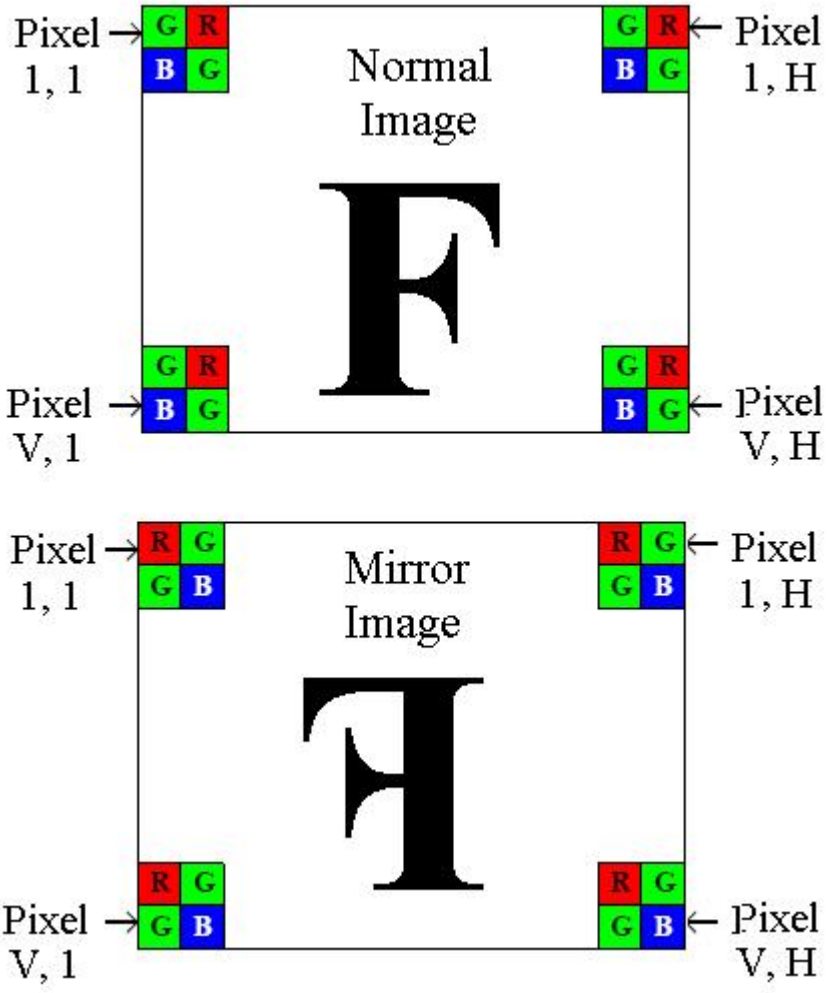


Figure 2.39 - Normal and Mirror Image

2.11 STATUS LED

The camera has a green LED, located on the back panel, which indicates the camera status and mode of operation.

- **LED is steady ON** – Normal operation. The user is expected to see a normal image coming out of the camera.
- **LED rapidly blinks with frequency ~ 5Hz** – indicates camera failure during camera setup. During camera power up this indicates an error in the camera boot up sequence. The user is expected to see a uniform gray screen. To restore the normal operation load the factory setting – refer the Camera Configuration section.
- **LED has one short blink every 3 seconds** – Test mode. The user is expected to see one of the test patterns.
- **LED has two short blinks every 3 seconds** – External trigger mode. The camera is waiting for an external trigger input.
- **LED has three short blinks every 3 seconds** – Test mode and External trigger mode enabled in the same time. The camera is waiting for an external trigger input and upon receiving the signal the user will see one of the test patterns.
- **LED blinks slowly with frequency ~ 0.3 Hz** – Long integration mode. The camera has to be kept steady to avoid image smear.
- **LED is OFF** – General error. The camera has no power or unexpected error occurred. To restore the camera operation, re-power the camera and load the factory settings.

2.12 TEST MODE

The camera can output three test images (two fixed and one moving), which can be used to verify the camera's general performance and connectivity to the frame grabber. This ensures that all the major modules in the hardware are working properly and that the connection between the frame grabber and the camera is synchronized (i.e., the camera parameters: # pixels, # lines, # bits, output mode, communication rate, etc. are properly configured). Figure 2.40 shows a diagonal gray scale variation for single and dual modes. Figure 2.41 shows gray scale vertical bars for single and dual modes. The motion test pattern is a diagonal gray scale variation similar to test pattern #1. The motion is in the vertical direction. The test mode does not exercise and verify the CCD's functionality.

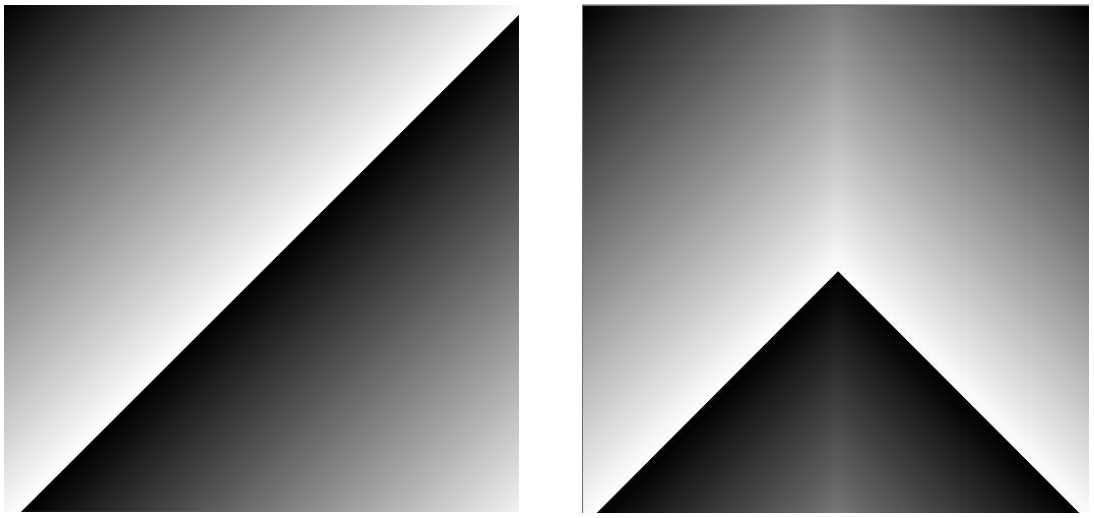


Figure 2.40 - Fixed Pattern #1: Single (left) and Dual (right) Modes

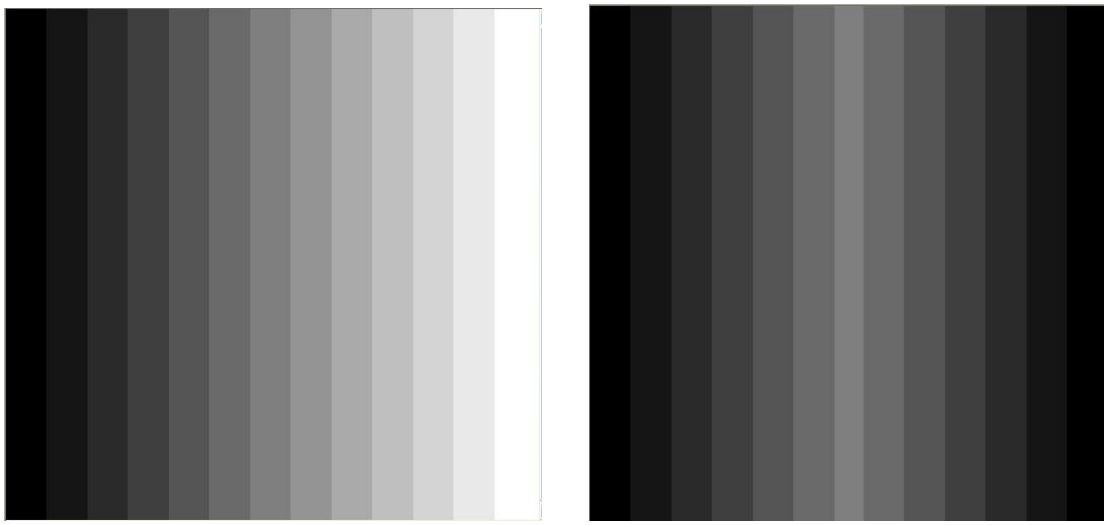
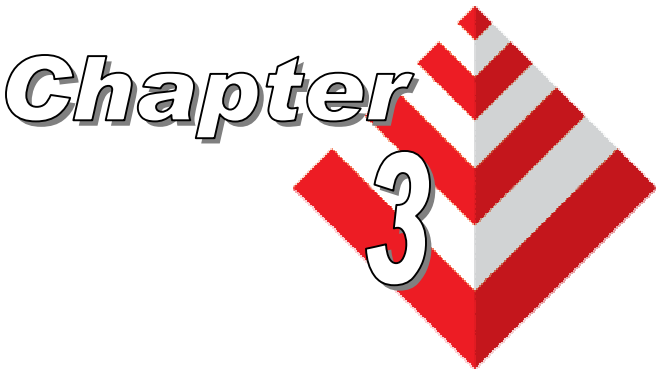


Figure 2.41 - Fixed Pattern #2: Single (left) and Dual (right) Modes



Camera Configuration

This chapter discusses how to configure the camera's operating parameters.

3.1 OVERVIEW

The IPX series of cameras are highly programmable and flexible. All of the camera's features and operating parameters can be controlled by the user. The user communicates with the camera using simple ASCII commands via the Camera Link's serial interface. All of the cameras resources (internal registers, video amplifiers and EEPROM) can be configured and monitored via this interface. The format of the serial interface is ASYNC with 8 data bits, 1 stop bit, no parity and no handshake. The interface operates at a rate of 9,600 bps. The interface is bi-directional with the user issuing 'commands' to the camera and the camera issuing 'responses' (either status or info) to the user. The camera's parameters can be programmed using the IPX Configurator graphical user interface.

3.2 CONFIGURATION MEMORY

The camera has a built-in configuration memory divided into 3 segments: ‘work-space’, ‘factory-space’ and ‘user-space’. The ‘work-space’ segment contains the current camera settings while the camera is powered-up and operational. All camera registers are located in this space. These registers can be programmed and retrieved via commands issued by the user. The workspace is RAM based and upon power down all camera registers are cleared. The ‘factory-space’ segment is ROM based, write protected and contains the default camera settings. This space is available for read operations only. The ‘user-space’ is non-volatile, EEPROM based and used to store the user defined configurations. Upon power up, the camera firmware loads the work-space registers from either the factory-space or user-space as determined by a ‘boot control’ register located in the configuration memory. The ‘boot control’ register can be programmed by the user (refer to Camera Configuration Section). The user can, at any time, instruct the camera to loads its workspace with the contents of either the ‘factory-space’ or ‘user-space’. The user can instruct the camera to save the current workspace settings only into ‘user-space’.

3.3 CAMERA REGISTERS

The camera work-space has 25 configuration registers for IPX-1M48 and 28 configuration registers for the rest of the cameras. All camera control registers are 8-bit and all AFE (analog front end) registers are 16-bit. Each register can be independently accessed. The general address map of IPX-1M48 camera registers is shown in Table 3.1. The general address map of IPX-VGA IPX-2M30, IPX-2M30H, IPX-4M15 and IPX-11M5 camera registers is shown in Tables 3.2. All registers marked with gray are not available for Write.

Device	Register	R/W	Address
Local Camera Control Registers	Camera Control 1	Read/Write	**00**
	Camera Control 2	Read/Write	**01**
	External Trigger Duration	Read/Write	**02**
	Reserved for Future use		**03**
	Vertical Window Top Lines Low	Read/Write	**04**
	Vertical Window Top Lines High	Read/Write	**05**
	Vertical Window Bottom Lines Low	Read/Write	**06**
	Vertical Window Bottom Lines High	Read/Write	**07**
	Shutter Time Select	Read/Write	**08**
	Reserved for Future use		**09**
	Long Integration Time Low	Read/Write	**0A**
	Pre-Exposure/Long Integration Time High	Read/Write	**0B**
	Strobe Position Select	Read/Write	**0C**
	Reserved for Future use		**0D**
	Horizontal Window Size Left	Read/Write	**0E**
	Horizontal Window Size Right	Read/Write	**0F**
Ch. 1 AFE Registers	Operation Low	Read/Write	**10**
	Operation High	Read/Write	**11**
	Gain Low	Read/Write	**12**
	Gain High	Read/Write	**13**
	Clamp Low	Read/Write	**14**
	Clamp High	Read/Write	**15**
	Control Low	Read/Write	**16**
	Control High	Read/Write	**17**
	Reserved for Future use		**18 : 1F**
Ch. 2 AFE Registers	Operation Low	Read/Write	**20**
	Operation High	Read/Write	**21**
	Gain Low	Read/Write	**22**

	Gain High	Read/Write	**23**
	Clamp Low	Read/Write	**24**
	Clamp High	Read/Write	**25**
	Control Low	Read/Write	**26**
	Control High	Read/Write	**27**
	Reserved for Future use		**28 : 2F**
Product ID	CCD FPGA Revision	Read Only	**30**
	Reserved for Future use		**31**
	DSP FPGA Revision	Read Only	**32**
	Reserved for Future use		**33**
	Reserved for Future use		**34 : 7F**
EEPROM Factory Settings	Local Camera Control Registers	Read Only	**80 : 8F**
	Ch.1 AFE Registers	Read Only	**90 : 9F**
	Ch. 2 AFE Registers	Read Only	**A0 : AF**
	MFG Data	Read Only	**B0 : BF**
EEPROM User Settings	Local Camera Control Registers	Read/Write	**C0 : CF**
	Ch.1 AFE Registers	Read/Write	**D0 : DF**
	Ch. 2 AFE Registers	Read/Write	**E0 : EF**
	Reserved for Future use		**F0 : FE**
BOOT	Boot Control	Read/Write	**FF**

Table 3.1. IPX-1M48 Camera work-space address map

Device	Register	R/W	Address
Local Camera Control Registers	Camera Control 1	Read/Write	**00**
	Camera Control 2	Read/Write	**01**
	External Trigger Duration	Read/Write	**02**
	Strobe Position Select High	Read/Write	**03**
	Vertical Window Top Lines Low	Read/Write	**04**
	Vertical Window Top Lines High	Read/Write	**05**
	Vertical Window Bottom Lines Low	Read/Write	**06**
	Vertical Window Bottom Lines High	Read/Write	**07**
	Shutter Time Select Low	Read/Write	**08**
	Shutter Time Select High	Read/Write	**09**
	Long Integration Time Low	Read/Write	**0A**
	Long Integration Time High	Read/Write	**0B**
	Strobe Position Select Low	Read/Write	**0C**

	Horizontal Window Size Left/Right High	Read/Write	**0D**
	Horizontal Window Size Left Low	Read/Write	**0E**
	Horizontal Window Size Right Low	Read/Write	**0F**
Ch. 1 AFE Registers	Operation Low	Read/Write	**10**
	Operation High	Read/Write	**11**
	Control Low	Read/Write	**12**
	Control High	Read/Write	**13**
	Clamp Low	Read/Write	**14**
	Clamp High	Read/Write	**15**
	Gain Low	Read	**16**
	Gain High	Read	**17**
	Reserved for Future use		**18 : 1F**
Ch. 2 AFE Registers	Operation Low	Read/Write	**20**
	Operation High	Read/Write	**21**
	Control Low	Read/Write	**22**
	Control High	Read/Write	**23**
	Clamp Low	Read/Write	**24**
	Clamp High	Read/Write	**25**
	Gain Low	Read/Write	**26**
	Gain High	Read/Write	**27**
	Reserved for Future use		**28 : 2F**
Product ID	CCD FPGA Revision	Read Only	**30**
	Reserved for Future use		**31**
	DSP FPGA Revision	Read Only	**32**
	Reserved for Future use		**33**
	Reserved for Future use		**34 : 7F**
EEPROM Factory Settings	Local Camera Control Registers	Read Only	**80 : 8F**
	Ch.1 AFE Registers	Read Only	**90 : 9F**
	Ch. 2 AFE Registers	Read Only	**A0 : AF**
	MFG Data	Read Only	**B0 : BF**
EEPROM User Settings	Local Camera Control Registers	Read/Write	**C0 : CF**
	Ch.1 AFE Registers	Read/Write	**D0 : DF**
	Ch. 2 AFE Registers	Read/Write	**E0 : EF**
	Reserved for Future use		**F0 : FE**
BOOT	Boot Control	Read/Write	**FF**

Table 3.2. IPX-VGA, 2M30/H, 4M15 and 11M5 Camera work-space address map.

3.4 REGISTERS AND EEPROM CONFIGURATION

3.4.1 Registers Configuration

In order to access the camera resources (internal registers, AFE registers and EEPROM) a sequence of characters have to be transmitted to the camera via the Camera Link serial interface. The format of the serial interface is ASYNC with 8 data bits, 1 stop bit, and no parity. The default baud rate is 9600 bps. Each camera control register can be updated independently. All AFE registers are 16-bit and therefore both low and high byte registers must be updated simultaneously. A delay of 1050 microsecond must be introduced after each command.
In order to write to any given **8-bit** camera register, the following sequence of characters, have to be sent to the camera:

8-bit register write:
1st character: 0xA5
2nd character: <register address>
3rd character: 0x5A
4th character: <register data>

In order to write to any given **16-bit** AFE register, the following sequence of characters, have to be sent to the camera. Please note that the upper and lower portion of the register must be updated simultaneously

16-bit register write:
1st character: 0xA5
2nd character: <register address low>
3rd character: 0x5A
4th character: <register data low>
5th character: 0xA5
6th character: <register address high>
7th character: 0x5A
8th character: <register data high>

In order to read from any given **8-bit** camera register, the following sequence of characters, have to be sent to the camera.

8-bit register read:
1st character: 0xA5
2nd character: <register address>
3rd character: 0x55
4th character: 0x55
The camera returns the low data character on the serial interface

In order to read from any given **16-bit** AFE register, the following sequence of characters, have to be sent to the camera.

16-bit register read:
1st character: 0xA5
2nd character: <register address low>
3rd character: 0x55
4th character: 0x55
The camera returns the low data character on the serial interface
5th character: 0xA5
6th character: <register address high>
7th character: 0x55
8th character: 0x55
The camera returns the high data character on the serial interface

Following the receipt of the above read sequence, the camera will transmit the requested register contents as a single character for each 8-bit register.

EXAMPLE:
To enable dual mode of operation the user has to change bit 'd1' of register 0x00 from logic-0 to logic-1. Please note that this is an 8-bit register. The corresponding script is:

```
# Camera Control register 0
# beginning of the script
uart_send 0xA5    # 'address' command
delay 1050        # delay of 1050 microseconds
uart_send 0x00    # register address 0x00
delay 1050
uart_send 0x5A    # 'write data' command
delay 1050
uart_send 0x02    # sets bit 'd1' to logic-1
delay 1050
# end of the script
```

Depending on the frame grabber manufacturer the function "uart_send" may have different syntax – refer to frame grabber manual for the correct function call. To prevent the serial buffer from being overwritten after each command, a delay of at least 1050 microsecond must be introduced.

3.4.2 EEPROM Configuration

To access the EEPROM the same sequence of characters have to be transmitted to the camera via the Camera Link serial interface. The format of the serial interface is the same: ASYNC with 8 data bits, 1 stop bit, and no parity. The default baud rate is 9600 bps. A delay of 10 milliseconds is required after each command. Only the user space is available for read and write. The factory space is read only.

3.5 IPX-VGA REGISTERS

3.5.1 IPX-VGA Control Registers

BOOT CONTROL: Address FF, factory default value 0x00.

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	Boot Mode

0 – Boot from Factory settings
1 – Boot from User settings

Table 3.3. IPX-VGA Boot Control Register.

CAMERA CONTROL 1: Address 0x00, factory default value 0x02.

D7	D6	D5	D4	D3	D2	D1	D0
Horizontal Window enable	Long Integration enable	Shutter enable	Vertical Window enable	Vertical Binning enable	Mirror Image enable	Dual Out enable	Strobe enable

0 - disable
1 - enable

Table 3.4. IPX-VGA Camera Control 1 Register.

CAMERA CONTROL 2: Address 0x01, factory default value 0x00.

D7	D6	D5	D4	D3	D2	D1	D0
8/10/12 bits 0	Test Mode 1	Test Mode 0	Gamma enable	8/10/12 bits 1	Horizontal Binning enable	CC1 Trigger enable	External Trigger enable

00 – 8 bit
01 – 10 bit
10 – 12 bit

00 - disable
01 - fixed image #1
10 - fixed image #2
11 - moving image

0 - disable
1 - enable

Table 3.5. IPX-VGA Camera Control 2 Register.

EXTERNAL TRIGGER DURATION: Address 0x02, factory default value 0x01.

External Trigger Duration								
D7	**D6**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**Value**
0	0	0	0	0	0	0	0	min
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	max

Table 3.6. IPX-VGA External Trigger Duration Register.

VERTICAL WINDOW TOP LINES: Address 0x04, factory default value 0x01.

Vertical Window Top Lines Low								
D7	**D6**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**Value**
0	0	0	0	0	0	0	0	min
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	max

Table 3.7. IPX-VGA Vertical Window Top Lines Register.

VERTICAL WINDOW BOTTOM LINES: Address 0x06, factory default value 0xF0.

Vertical Window Bottom Lines Low								
D7	**D6**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**Value**
0	0	0	0	0	0	0	0	min
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	max

Table 3.8. IPX-VGA Vertical Window Bottom Lines Register.

SHUTTER TIME SELECT: Address 0x08, factory default value 0x01.

Shutter Time Select Low								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Value**
0	0	0	0	0	0	0	0	min
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	max

Table 3.9. IPX-VGA Shutter Time Select Register.

LONG INTEGRATION TIME LOW: Address 0x0A, factory default value 0x01.

Long Integration Time Low								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Value**
0	0	0	0	0	0	0	0	min
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	max

Table 3.10a. IPX-VGA Long Integration Time Low Register.

PRE-EXPOSURE/LONG INTEGRATION TIME HIGH: Address 0x0B, factory default value 0x00. This register shares pre-exposure and long integration high.

Pre-Exposure						Long Integration Time High		
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Value**
PE D5	PE D4	PE D3	PE D2	PE D1	PE D0	LIT D9	LIT D8	
0	0	0	0	0	0	0	0	min
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	max

Table 3.10b. IPX-VGA Pre-Exposure/Long Integration Time High Register.

STROBE POSITION SELECT: Address 0x0C, factory default value 0x01.

Strobe Position Select Low								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Value**
0	0	0	0	0	0	0	0	min
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	max

Table 3.11. IPX-VGA Strobe Position Select Low Register.

HORIZONTAL WINDOW SIZE LEFT: Address 0x0E, factory default value 0x01.

Horizontal Window Size Left Low								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Value**
0	0	0	0	0	0	0	0	min
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	max

Table 3.12. IPX-VGA Horizontal Window Size Left Register.

HORIZONTAL WINDOW SIZE RIGHT: Address 0x0F, factory default value 0x01.

Horizontal Window Size Right Low								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Value**
0	0	0	0	0	0	0	0	min
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	max

Table 3.13. IPX-VGA Horizontal Window Size Right Register.

3.5.2 IPX-VGA Video (AFE) Registers

AFE OPERATION LOW: Address (0x10 ch1; 0x20 ch2), factory default value 0x48.

Operation Low							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	1	0	0	1	0	0	0

Table 3.14a. IPX-VGA AFE Operation Low Register.

AFE OPERATION HIGH: Address (0x 11 ch1; 0x21 ch2), factory default value 0x00.

Operation High							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	0	0	0	0	0	0	0

Table 3.14b. IPX-VGA AFE Operation High Register.

AFE CONTROL LOW: Address (0x12 ch1; 0x22 ch2), factory default value 0x04.

AFE Control Low							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	0	0	0	0	1	0	0

Table 3.15a. IPX-VGA AFE Control Low Register.

AFE CONTROL HIGH: Address (0x13 ch1; 0x23 ch2), factory default value 0x00.

AFE Control High							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	0	0	0	0	0	0	0

Table 3.15b. IPX-VGA AFE Control High Register.

AFE CLAMP LOW: Address (0x14 ch1; 0x24 ch2), factory default value 0x00.

AFE Clamp Low								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Value**
0	0	0	0	0	0	0	0	min
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	max

Table 3.16a. IPX-VGA AFE Clamp Low Register.

AFE CLAMP HIGH: Address (0x15 ch1; 0x25 ch2), factory default value 0x00.

AFE Clamp High								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Value**
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0

Table 3.16b. IPX-VGA AFE Clamp High Register.

AFE GAIN LOW: Address (0x16 ch1; 0x26 ch2), factory default value 0xAA.

AFE Gain Low								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Value**
0	0	0	0	0	0	0	0	min
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	max

Table 3.17a. IPX-VGA AFE Gain Low Register.

AFE GAIN HIGH: Address (0x17 ch1; 0x27 ch2), factory default value 0x00.

AFE Gain High								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Value**
0	0	0	0	0	0	0	0	min
0	0	0	0	0	0	:	:	:
0	0	0	0	0	0	1	1	max

Table 3.17b. IPX-VGA AFE Gain High Register.

3.5.3 IPX-VGA Manufacturing Data Registers

MANUFACTURING DATA: Address (0xB0 to BF)

Address	Contents	Type	Range
B0	Assembly Part Number and Revision Number	HEX	0x00 : 0xFF
B1		HEX	0x00 : 0xFF
B2		HEX	0x00 : 0xFF
B3		HEX	0x00 : 0xFF
B4		ASCII	A : Z, 0: 9
B5		ASCII	A : Z, 0: 9
B6		ASCII	A : Z, 0: 9
B7	Assembly Serial Number	HEX	0x00 : 0xFF
B8		HEX	0x00 : 0xFF
B9		HEX	0x00 : 0xFF
BA	CCD Serial Number	HEX	0x00 : 0xFF
BB		HEX	0x00 : 0xFF
BC		HEX	0x00 : 0xFF
BD	Date of Mfg.	HEX	0x00 : 0xFF
BE		HEX	0x00 : 0xFF
BF		HEX	0x00 : 0xFF

Table 3.18. IPX-VGA Manufacturing Data Registers

3.6 IPX-1M48 REGISTERS

3.6.1 IPX-1M48 Control Registers

BOOT CONTROL: Address FF, factory default value 0x00.

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	Boot Mode

0 – Boot from Factory settings
1 – Boot from User settings

Table 3.19. IPX-1M48 Boot Control Register.

CAMERA CONTROL 1: Address 0x00, factory default value 0x02.

D7	D6	D5	D4	D3	D2	D1	D0
Horizontal Window enable	Long Integration enable	Shutter enable	Vertical Window enable	Vertical Binning enable	Mirror Image enable	Dual Out enable	Strobe enable

0 - disable
1 - enable

Table 3.20. IPX-1M48 Camera Control 1 Register.

CAMERA CONTROL 2: Address 0x01, factory default value 0x00.

D7	D6	D5	D4	D3	D2	D1	D0
8/10/12 bits 0	Test Mode 1	Test Mode 0	Gamma enable	8/10/12 bits 1	Horizontal Binning enable	CC1 Trigger enable	External Trigger enable

00 – 8 bit
01 – 10 bit
10 – 12 bit

00 - disable
01 - fixed image #1
10 - fixed image #2
11 - moving image

0 - disable
1 - enable

Table 3.21. IPX-1M48 Camera Control 2 Register.

EXTERNAL TRIGGER DURATION: Address 0x02, factory default value 0x01.

External Trigger Duration								
D7	**D6**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**Value**
0	0	0	0	0	0	0	0	min
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	max

Table 3.22. IPX-1M48 External Trigger Duration Register.

VERTICAL WINDOW TOP LINES LOW: Address 0x04, factory default value 0x01.

Vertical Window Top Lines Low								
D7	**D6**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**Value**
0	0	0	0	0	0	0	0	min
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	max

Table 3.23a. IPX-1M48 Vertical Window Top Lines Low Register.

VERTICAL WINDOW TOP LINES HIGH: Address 0x05, factory default value 0x00.

Vertical Window Top Lines High								
D7	**D6**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**Value**
0	0	0	0	0	0	0	0	min
0	0	0	0	0	0	:	:	:
0	0	0	0	0	0	1	1	max

Table 3.23b. IPX-1M48 Vertical Window Top Lines High Register.

VERTICAL WINDOW BOTTOM LINES LOW: Address 0x06, factory default value 0xEC.

Vertical Window Bottom Lines Low								
D7	**D6**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**Value**
0	0	0	0	0	0	0	0	min
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	max

Table 3.24a. IPX-1M48 Vertical Window Bottom Lines Low Register.

VERTICAL WINDOW BOTTOM LINES HIGH: Address 0x07, factory default value 0x03.

Vertical Window Bottom Lines High								
D7	**D6**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**Value**
0	0	0	0	0	0	0	0	min
0	0	0	0	0	0	:	:	:
0	0	0	0	0	0	1	1	max

Table 3.24b. IPX-1M48 Vertical Window Bottom Lines High Register.

SHUTTER TIME SELECT: Address 0x08, factory default value 0x01.

Shutter Time Select								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Value**
0	0	0	0	0	0	0	0	min
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	max

Table 3.25. IPX-1M48 Shutter Time Select Register.

LONG INTEGRATION TIME LOW: Address 0x0A, factory default value 0x01.

Long Integration Time Low								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Value**
0	0	0	0	0	0	0	0	min
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	max

Table 3.26a. IPX-1M48 Long Integration Time Low Register.

PRE-EXPOSURE/LONG INTEGRATION TIME HIGH: Address 0x0B, factory default value 0x00. This register shares pre-exposure and long integration high.

Pre-Exposure						Long Integration Time High		
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Value**
PE D5	PE D4	PE D3	PE D2	PE D1	PE D0	LIT D9	LIT D8	
0	0	0	0	0	0	0	0	min
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	max

Table 3.26b. IPX-1M48 Pre-Exposure/Long Integration Time High Register.

STROBE POSITION SELECT: Address 0x0C, factory default value 0x01.

Strobe Position Select								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Value**
0	0	0	0	0	0	0	0	min
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	max

Table 3.27. IPX-1M48 Strobe Position Select Register.

HORIZONTAL WINDOW SIZE LEFT: Address 0x0E, factory default value 0x01.

Horizontal Window Size Left								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Value**
0	0	0	0	0	0	0	0	min
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	max

Table 3.28. IPX-1M48 Horizontal Window Size Left Register.

HORIZONTAL WINDOW SIZE RIGHT: Address 0x0F, factory default value 0x01.

Horizontal Window Size Right								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Value**
0	0	0	0	0	0	0	0	min
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	max

Table 3.29. IPX-1M48 Horizontal Window Size Right Register.

3.6.2 IPX-1M48 Video (AFE) Registers

AFE OPERATION LOW: Address (0x10 ch1; 0x20 ch2), factory default value 0x83.

Operation Low							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	0	CL	0	0	0	1	1

CLAMP
0 – enable, 1 - disable

Table 3.30a. IPX-1M48 AFE Operation Low Register.

AFE OPERATION HIGH: Address (0x 11 ch1; 0x21 ch2), factory default value 0x00.

Operation High							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	0	0	0	0	0	0	0

Table 3.30b. IPX-1M48 AFE Operation High Register.

AFE GAIN LOW: Address (0x12 ch1; 0x22 ch2), factory default value 0xAA.

AFE Gain Low								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Value**
0	0	0	0	0	0	0	0	min
:	**:**	**:**	**:**	**:**	**:**	**:**	**:**	**:**
1	1	1	1	1	1	1	1	max

Table 3.31a. IPX-1M48 AFE Gain Low Register.

AFE GAIN HIGH: Address (0x13 ch1; 0x23 ch2), factory default value 0x00.

AFE Gain High								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Value**
0	0	0	0	0	0	0	0	min
0	0	0	0	0	0	**:**	**:**	**:**
0	0	0	0	0	0	1	1	max

Table 3.31b. IPX-1M48 AFE Gain High Register.

AFE CLAMP LOW: Address (0x14 ch1; 0x24 ch2), factory default value 0x00.

AFE Clamp Low								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Value**
0	0	0	0	0	0	0	0	min
:	**:**	**:**	**:**	**:**	**:**	**:**	**:**	**:**
1	1	1	1	1	1	1	1	max

Table 3.32a. IPX-1M48 AFE Clamp Low Register.

AFE CLAMP HIGH: Address (0x15 ch1; 0x25 ch2), factory default value 0x00.

AFE Clamp High								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Value**
0	0	0	0	0	0	0	0	min
0	0	0	0	0	0	0	0	:
0	0	0	0	0	0	0	0	max

Table 3.32b. IPX-1M48 AFE Clamp High Register.

AFE CONTROL LOW: Address (0x16 ch1; 0x26 ch2), factory default value 0x00.

AFE Control Low							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	0	0	0	0	0	0	0

Table 3.33a. IPX-1M48 AFE Control Low Register.

AFE CONTROL HIGH: Address (0x17 ch1; 0x27 ch2), factory default value 0x00.

AFE Control High							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	0	0	0	0	0	0	0

Table 3.33b. IPX-1M48 AFE Control High Register.

3.6.3 IPX-1M48 Manufacturing Data Registers

MANUFACTURING DATA: Address (0xB0 to BF)

Address	Contents	Type	Range
B0	Assembly Part Number and Revision Number	HEX	0x00 : 0xFF
B1		HEX	0x00 : 0xFF
B2		HEX	0x00 : 0xFF
B3		HEX	0x00 : 0xFF
B4		ASCII	A : Z, 0: 9
B5		ASCII	A : Z, 0: 9
B6		ASCII	A : Z, 0: 9
B7	Assembly Serial Number	HEX	0x00 : 0xFF
B8		HEX	0x00 : 0xFF
B9		HEX	0x00 : 0xFF
BA	CCD Serial Number	HEX	0x00 : 0xFF
BB		HEX	0x00 : 0xFF
BC		HEX	0x00 : 0xFF
BD	Date of Mfg.	HEX	0x00 : 0xFF
BE		HEX	0x00 : 0xFF
BF		HEX	0x00 : 0xFF

Table 3.34. IPX-1M48 Manufacturing Data Registers

3.7 IPX-2M30 REGISTER

3.7.1 IPX-2M30 Control Registers

BOOT CONTROL: Address FF, factory default value 0x00.

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	Boot Mode

0 – Boot from Factory settings
1 – Boot from User settings

Table 3.35. IPX-2M30 Boot Control Register.

CAMERA CONTROL 1: Address 0x00, factory default value 0x02.

D7	D6	D5	D4	D3	D2	D1	D0
Horizontal Window enable	Long Integration enable	Shutter enable	Vertical Window enable	Vertical Binning enable	Mirror Image enable	Dual Out enable	Strobe enable

0 - disable
1 - enable

Table 3.36. IPX-2M30 Camera Control 1 Register.

CAMERA CONTROL 2: Address 0x01, factory default value 0x00.

D7	D6	D5	D4	D3	D2	D1	D0
8/10/12 bits 0	Test Mode 1	Test Mode 0	Gamma enable	8/10/12 bits 1	Horizontal Binning enable	CC1 Trigger enable	External Trigger enable

00 – 8 bit
01 – 10 bit
10 – 12 bit

00 - disable
01 - fixed image #1
10 - fixed image #2
11 - moving image

0 - disable
1 - enable

Table 3.37. IPX-2M30 Camera Control 2 Register.

EXTERNAL TRIGGER DURATION: Address 0x02, factory default value 0x01.

External Trigger Duration								
D7	**D6**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**Value**
0	0	0	0	0	0	0	0	min
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	max

Table 3.38. IPX-2M30 External Trigger Duration Register.

VERTICAL WINDOW TOP LINES LOW: Address 0x04, factory default value 0x01.

Vertical Window Top Lines Low								
D7	**D6**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**Value**
0	0	0	0	0	0	0	0	min
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	max

Table 3.39a. IPX-2M30 Vertical Window Top Lines Low Register.

VERTICAL WINDOW TOP LINES HIGH: Address 0x05, factory default value 0x00.

Vertical Window Top Lines High								
D7	**D6**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**Value**
0	0	0	0	0	0	0	0	min
0	0	0	0	0	:	:	:	:
0	0	0	0	0	1	1	1	max

Table 3.39b. IPX-2M30 Vertical Window Top Lines High Register.

VERTICAL WINDOW BOTTOM LINES LOW: Address 0x06, factory default value 0x40.

Vertical Window Bottom Lines Low								
D7	**D6**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**Value**
0	0	0	0	0	0	0	0	min
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	max

Table 3.40a. IPX-2M30 Vertical Window Bottom Lines Low Register.

VERTICAL WINDOW BOTTOM LINES HIGH: Address 0x07, factory default value 0x06.

Vertical Window Bottom Lines High								
D7	**D6**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**Value**
0	0	0	0	0	0	0	0	min
0	0	0	0	0	:	:	:	:
0	0	0	0	0	1	1	1	max

Table 3.40b. IPX-2M30 Vertical Window Bottom Lines High Register.

SHUTTER TIME SELECT LOW: Address 0x08, factory default value 0x01.

Shutter Time Select Low								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Value**
0	0	0	0	0	0	0	0	min
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	max

Table 3.41a. IPX-2M30 Shutter Time Select Low Register.

SHUTTER TIME SELECT HIGH: Address 0x09, factory default value 0x00.

Shutter Time Select High								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Value**
0	0	0	0	0	0	0	0	min
0	0	0	0	0	:	:	:	:
0	0	0	0	0	1	1	1	max

Table 3.41b. IPX-2M30 Shutter Time Select High Register.

LONG INTEGRATION TIME LOW: Address 0x0A, factory default value 0x01.

Long Integration Time Low								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Value**
0	0	0	0	0	0	0	0	min
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	max

Table 3.42a. IPX-2M30 Long Integration Time Low Register.

PRE-EXPOSURE/LONG INTEGRATION TIME HIGH: Address 0x0B, factory default value 0x00. This register shares pre-exposure and long integration high.

Pre-Exposure						Long Integration Time High		
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Value**
PE D5	PE D4	PE D3	PE D2	PE D1	PE D0	LIT D9	LIT D8	
0	0	0	0	0	0	0	0	min
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	max

Table 3.42b. IPX-2M30 Pre-Exposure/Long Integration Time High Register.

STROBE POSITION SELECT LOW: Address 0x0C, factory default value 0x01.

Strobe Position Select Low								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Value**
0	0	0	0	0	0	0	0	min
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	max

Table 3.43a. IPX-2M30 Strobe Position Select Low Register.

STROBE POSITION SELECT HIGH: Address 0x03, factory default value 0x00.

Strobe Position Select High								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Value**
0	0	0	0	0	0	0	0	min
0	0	0	0	0	:	:	:	:
0	0	0	0	0	1	1	1	max

Table 3.43b. IPX-2M30 Strobe Position Select High Register.

HORIZONTAL WINDOW SIZE LEFT LOW: Address 0x0E, factory default value 0x01.

Horizontal Window Size Left Low								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Value**
0	0	0	0	0	0	0	0	min
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	max

Table 3.44a. IPX-2M30 Horizontal Window Size Left Low Register.

HORIZONTAL WINDOW SIZE RIGHT LOW: Address 0x0F, factory default value 0x01.

Horizontal Window Size Right Low								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Value**
0	0	0	0	0	0	0	0	min
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	max

Table 3.44b. IPX-2M30 Horizontal Window Size Right Low Register.

HORIZONTAL WINDOW SIZE LEFT/RIGHT HIGH: Address 0x0D, factory default value 0x00. This register shares horizontal window left high and horizontal window right high.

Horizontal Window Size L/R High								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Value**
0	0	0	0	0	0	0	0	min
0	0	:	:	0	0	:	:	:
0	0	1	1	0	0	1	1	max

Table 3.45. IPX-2M30 Horizontal Window Size Left/Right High Register.

3.7.2 IPX-2M30 Video (AFE) Registers

AFE OPERATION LOW: Address (0x10 ch1; 0x20 ch2), factory default value 0x48.

Operation Low							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	1	0	0	1	0	0	0

Table 3.46a. IPX-2M30 AFE Operation Low Register.

AFE OPERATION HIGH: Address (0x 11 ch1; 0x21 ch2), factory default value 0x00.

Operation High							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	0	0	0	0	0	0	0

Table 3.46b. IPX-2M30 AFE Operation High Register.

AFE CONTROL LOW: Address (0x12 ch1; 0x22 ch2), factory default value 0x04.

AFE Control Low							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	0	0	0	0	1	0	0

Table 3.47a. IPX-2M30 AFE Control Low Register.

AFE CONTROL HIGH: Address (0x13 ch1; 0x23 ch2), factory default value 0x00.

AFE Control High							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	0	0	0	0	0	0	0

Table 3.47b. IPX-2M30 AFE Control High Register.

AFE CLAMP LOW: Address (0x14 ch1; 0x24 ch2), factory default value 0x00.

AFE Clamp Low								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Value**
0	0	0	0	0	0	0	0	min
:	**:**	**:**	**:**	**:**	**:**	**:**	**:**	**:**
1	1	1	1	1	1	1	1	max

Table 3.48a. IPX-2M30 AFE Clamp Low Register.

AFE CLAMP HIGH: Address (0x15 ch1; 0x25 ch2), factory default value 0x00.

AFE Clamp High								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Value**
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0

Table 3.48b. IPX-2M30 AFE Clamp High Register.

AFE GAIN LOW: Address (0x16 ch1; 0x26 ch2), factory default value 0xAA.

AFE Gain Low								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Value**
0	0	0	0	0	0	0	0	min
:	**:**	**:**	**:**	**:**	**:**	**:**	**:**	**:**
1	1	1	1	1	1	1	1	max

Table 3.49a. IPX-2M30 AFE Gain Low Register.

AFE GAIN HIGH: Address (0x17 ch1; 0x27 ch2), factory default value 0x00.

AFE Gain High								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Value**
0	0	0	0	0	0	0	0	min
0	0	0	0	0	0	**:**	**:**	**:**
0	0	0	0	0	0	1	1	max

Table 3.49b. IPX-2M30 AFE Gain High Register.

3.7.3 IPX-2M30 Manufacturing Data Registers

MANUFACTURING DATA: Address (0xB0 to BF)

Address	Contents	Type	Range
B0	Assembly Part Number and Revision Number	HEX	0x00 : 0xFF
B1		HEX	0x00 : 0xFF
B2		HEX	0x00 : 0xFF
B3		HEX	0x00 : 0xFF
B4		ASCII	A : Z, 0: 9
B5		ASCII	A : Z, 0: 9
B6		ASCII	A : Z, 0: 9
B7	Assembly Serial Number	HEX	0x00 : 0xFF
B8		HEX	0x00 : 0xFF
B9		HEX	0x00 : 0xFF
BA	CCD Serial Number	HEX	0x00 : 0xFF
BB		HEX	0x00 : 0xFF
BC		HEX	0x00 : 0xFF
BD	Date of Mfg.	HEX	0x00 : 0xFF
BE		HEX	0x00 : 0xFF
BF		HEX	0x00 : 0xFF

Table 3.50. IPX-2M30 Manufacturing Data Registers

3.8 IPX-2M30H REGISTERS

3.8.1 IPX-2M30H Control Registers

BOOT CONTROL: Address FF, factory default value 0x00.

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	Boot Mode

0 – Boot from Factory settings
1 – Boot from User settings

Table 3.51. IPX-2M30H Boot Control Register.

CAMERA CONTROL 1: Address 0x00, factory default value 0x02.

D7	D6	D5	D4	D3	D2	D1	D0
Horizontal Window enable	Long Integration enable	Shutter enable	Vertical Window enable	Vertical Binning enable	Mirror Image enable	Dual Out enable	Strobe enable

0 - disable
1 - enable

Table 3.52. IPX-2M30H Camera Control 1 Register.

CAMERA CONTROL 2: Address 0x01, factory default value 0x00.

D7	D6	D5	D4	D3	D2	D1	D0
8/10/12 bits 0	Test Mode 1	Test Mode 0	Gamma enable	8/10/12 bits 1	Horizontal Binning enable	CC1 Trigger enable	External Trigger enable

00 – 8 bit
01 – 10 bit
10 – 12 bit

00 - disable
01 - fixed image #1
10 - fixed image #2
11 - moving image

0 - disable
1 - enable

Table 3.53. IPX-2M30H Camera Control 2 Register.

EXTERNAL TRIGGER DURATION: Address 0x02, factory default value 0x01.

External Trigger Duration								
D7	**D6**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**Value**
0	0	0	0	0	0	0	0	min
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	max

Table 3.54. IPX-2M30H External Trigger Duration Register.

SHUTTER TIME SELECT LOW: Address 0x08, factory default value 0x01.

Shutter Time Select Low								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Value**
0	0	0	0	0	0	0	0	min
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	max

Table 3.55. IPX-2M30H Shutter Time Select Low Register.

SHUTTER TIME SELECT HIGH: Address 0x09, factory default value 0x00.

Shutter Time Select High								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Value**
0	0	0	0	0	0	0	0	min
0	0	0	0	0	:	:	:	:
0	0	0	0	0	1	1	1	max

Table 3.56. IPX-2M30H Shutter Time Select High Register.

LONG INTEGRATION TIME LOW: Address 0x0A, factory default value 0x01.

Long Integration Time Low								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Value**
0	0	0	0	0	0	0	0	min
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	max

Table 3.57. IPX-2M30H Long Integration Time Low Register.

PRE-EXPOSURE/LONG INTEGRATION TIME HIGH: Address 0x0B, factory default value 0x00. This register shares pre-exposure and long integration high.

Pre-Exposure						Long Integration Time High		
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Value**
PE D5	PE D4	PE D3	PE D2	PE D1	PE D0	LIT D9	LIT D8	
0	0	0	0	0	0	0	0	min
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	max

Table 3.58. IPX-2M30H Pre-Exposure/Long Integration Time High Register.

STROBE POSITION SELECT LOW: Address 0x0C, factory default value 0x01.

Strobe Position Select Low								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Value**
0	0	0	0	0	0	0	0	min
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	max

Table 3.59a. IPX-2M30H Strobe Position Select Low Register.

STROBE POSITION SELECT HIGH: Address 0x03, factory default value 0x00.

Strobe Position Select High								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Value**
0	0	0	0	0	0	0	0	min
0	0	0	0	0	:	:	:	:
0	0	0	0	0	1	1	1	max

Table 3.59b. IPX-2M30H Strobe Position Select High Register.

HORIZONTAL WINDOW SIZE LEFT LOW: Address 0x0E, factory default value 0x01.

Horizontal Window Size Left Low								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Value**
0	0	0	0	0	0	0	0	min
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	max

Table 3.60a. IPX-2M30H Horizontal Window Size Left Low Register.

HORIZONTAL WINDOW SIZE RIGHT LOW: Address 0x0F, factory default value 0x01.

Horizontal Window Size Right Low								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Value**
0	0	0	0	0	0	0	0	min
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	max

Table 3.60b. IPX-2M30H Horizontal Window Size Right Low Register.

HORIZONTAL WINDOW SIZE LEFT/RIGHT HIGH: Address 0x0D, factory default value 0x00. This register shares horizontal window left high and horizontal window right high.

Horizontal Window Size L/R High								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Value**
0	0	0	0	0	0	0	0	min
0	0	:	:	0	0	:	:	:
0	0	1	1	0	0	1	1	max

Table 3.61. IPX-2M30H Horizontal Window Size Left/Right High Register.

3.8.2 IPX-2M30H Video (AFE) Registers

AFE OPERATION LOW: Address (0x10 ch1; 0x20 ch2), factory default value 0x48.

Operation Low							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	1	0	0	1	0	0	0

Table 3.62a. IPX-2M30H AFE Operation Low Register.

AFE OPERATION HIGH: Address (0x 11 ch1; 0x21 ch2), factory default value 0x00.

Operation High							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	0	0	0	0	0	0	0

Table 3.62b. IPX-2M30H AFE Operation High Register.

AFE CONTROL LOW: Address (0x12 ch1; 0x22 ch2), factory default value 0x04.

AFE Control Low							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	0	0	0	0	1	0	0

Table 3.63a. IPX-2M30H AFE Control Low Register.

AFE CONTROL HIGH: Address (0x13 ch1; 0x23 ch2), factory default value 0x00.

AFE Control High							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	0	0	0	0	0	0	0

Table 3.63b. IPX-2M30H AFE Control High Register.

AFE CLAMP LOW: Address (0x14 ch1; 0x24 ch2), factory default value 0x00.

AFE Clamp Low								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Value**
0	0	0	0	0	0	0	0	min
:	**:**	**:**	**:**	**:**	**:**	**:**	**:**	**:**
1	1	1	1	1	1	1	1	max

Table 3.64a. IPX-2M30H AFE Clamp Low Register.

AFE CLAMP HIGH: Address (0x15 ch1; 0x25 ch2), factory default value 0x00.

AFE Clamp High								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Value**
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0

Table 3.64b. IPX-2M30H AFE Clamp High Register.

AFE GAIN LOW: Address (0x16 ch1; 0x26 ch2), factory default value 0xAA.

AFE Gain Low								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Value**
0	0	0	0	0	0	0	0	min
:	**:**	**:**	**:**	**:**	**:**	**:**	**:**	**:**
1	1	1	1	1	1	1	1	max

Table 3.65a. IPX-2M30H AFE Gain Low Register.

AFE GAIN HIGH: Address (0x17 ch1; 0x27 ch2), factory default value 0x00.

AFE Gain High								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Value**
0	0	0	0	0	0	0	0	min
0	0	0	0	0	0	**:**	**:**	**:**
0	0	0	0	0	0	1	1	max

Table 3.65b. IPX-2M30H AFE Gain High Register.

3.8.3 IPX-2M30H Manufacturing Data Registers

MANUFACTURING DATA: Address (0xB0 to BF)

Address	Contents	Type	Range
B0	Assembly Part Number and Revision Number	HEX	0x00 : 0xFF
B1		HEX	0x00 : 0xFF
B2		HEX	0x00 : 0xFF
B3		HEX	0x00 : 0xFF
B4		ASCII	A : Z, 0: 9
B5		ASCII	A : Z, 0: 9
B6		ASCII	A : Z, 0: 9
B7	Assembly Serial Number	HEX	0x00 : 0xFF
B8		HEX	0x00 : 0xFF
B9		HEX	0x00 : 0xFF
BA	CCD Serial Number	HEX	0x00 : 0xFF
BB		HEX	0x00 : 0xFF
BC		HEX	0x00 : 0xFF
BD	Date of Mfg.	HEX	0x00 : 0xFF
BE		HEX	0x00 : 0xFF
BF		HEX	0x00 : 0xFF

Table 3.66. IPX-2M30H Manufacturing Data Registers

3.9 IPX-4M15 REGISTERS

3.9.1 IPX-4M15 Control Registers

BOOT CONTROL: Address FF, factory default value 0x00.

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	Boot Mode

0 – Boot from Factory settings
1 – Boot from User settings

Table 3.67. IPX-4M15 Boot Control Register.

CAMERA CONTROL 1: Address 0x00, factory default value 0x02.

D7	D6	D5	D4	D3	D2	D1	D0
Horizontal Window enable	Long Integration enable	Shutter enable	Vertical Window enable	Vertical Binning enable	Mirror Image enable	Dual Out enable	Strobe enable

0 - disable
1 - enable

Table 3.68. IPX-4M15 Camera Control 1 Register.

CAMERA CONTROL 2: Address 0x01, factory default value 0x00.

D7	D6	D5	D4	D3	D2	D1	D0
8/10/12 bits 0	Test Mode 1	Test Mode 0	Gamma enable	8/10/12 bits 1	Horizontal Binning enable	CC1 Trigger enable	External Trigger enable

00 – 8 bit
01 – 10 bit
10 – 12 bit

00 - disable
01 - fixed image #1
10 - fixed image #2
11 - moving image

0 - disable
1 - enable

Table 3.69. IPX-4M15 Camera Control 2 Register.

EXTERNAL TRIGGER DURATION: Address 0x02, factory default value 0x01.

External Trigger Duration								
D7	**D6**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**Value**
0	0	0	0	0	0	0	0	min
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	max

Table 3.70. IPX-4M15 External Trigger Duration Register.

VERTICAL WINDOW TOP LINES LOW: Address 0x04, factory default value 0x01.

Vertical Window Top Lines Low								
D7	**D6**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**Value**
0	0	0	0	0	0	0	0	min
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	max

Table 3.71a. IPX-4M15 Vertical Window Top Lines Low Register.

VERTICAL WINDOW TOP LINES HIGH: Address 0x05, factory default value 0x00.

Vertical Window Top Lines High								
D7	**D6**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**Value**
0	0	0	0	0	0	0	0	min
0	0	0	0	:	:	:	:	:
0	0	0	0	1	1	1	1	max

Table 3.71b. IPX-4M15 Vertical Window Top Lines High Register.

VERTICAL WINDOW BOTTOM LINES LOW: Address 0x06, factory default value 0x00.

Vertical Window Bottom Lines Low								
D7	**D6**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**Value**
0	0	0	0	0	0	0	0	min
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	max

Table 3.72a. IPX-4M15 Vertical Window Bottom Lines Low Register.

VERTICAL WINDOW BOTTOM LINES HIGH: Address 0x07, factory default value 0x08.

Vertical Window Bottom Lines High								
D7	**D6**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**Value**
0	0	0	0	0	0	0	0	min
0	0	0	0	:	:	:	:	:
0	0	0	0	1	1	1	1	max

Table 3.72b. IPX-4M15 Vertical Window Bottom Lines High Register.

SHUTTER TIME SELECT LOW: Address 0x08, factory default value 0x01.

Shutter Time Select Low								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Value**
0	0	0	0	0	0	0	0	min
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	max

Table 3.73a. IPX-4M15 Shutter Time Select Low Register.

SHUTTER TIME SELECT HIGH: Address 0x09, factory default value 0x00.

Shutter Time Select High								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Value**
0	0	0	0	0	0	0	0	min
0	0	0	0	:	:	:	:	:
0	0	0	0	1	1	1	1	max

Table 3.73b. IPX-4M15 Shutter Time Select High Register.

LONG INTEGRATION TIME LOW: Address 0x0A, factory default value 0x01.

Long Integration Time Low								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Value**
0	0	0	0	0	0	0	0	min
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	max

Table 3.74a. IPX-4M15 Long Integration Time Low Register.

PRE-EXPOSURE/LONG INTEGRATION TIME HIGH: Address 0x0B, factory default value 0x00. This register shares pre-exposure and long integration high.

Pre-Exposure						Long Integration Time High		
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Value**
PE D5	PE D4	PE D3	PE D2	PE D1	PE D0	LIT D9	LIT D8	
0	0	0	0	0	0	0	0	min
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	max

Table 3.74b. IPX-4M15 Pre-Exposure/Long Integration Time High Register.

STROBE POSITION SELECT LOW: Address 0x0C, factory default value 0x01.

Strobe Position Select Low								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Value**
0	0	0	0	0	0	0	0	min
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	max

Table 3.75a. IPX-4M15 Strobe Position Select Low Register.

STROBE POSITION SELECT HIGH: Address 0x03, factory default value 0x00.

Strobe Position Select High								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Value**
0	0	0	0	0	0	0	0	min
0	0	0	0	:	:	:	:	:
0	0	0	0	1	1	1	1	max

Table 3.75b. IPX-4M15 Strobe Position Select High Register.

HORIZONTAL WINDOW SIZE LEFT LOW: Address 0x0E, factory default value 0x01.

Horizontal Window Size Left Low								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Value**
0	0	0	0	0	0	0	0	min
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	max

Table 3.76a. IPX-4M15 Horizontal Window Size Left Low Register.

HORIZONTAL WINDOW SIZE RIGHT LOW: Address 0x0F, factory default value 0x01.

Horizontal Window Size Right Low								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Value**
0	0	0	0	0	0	0	0	min
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	max

Table 3.76b. IPX-4M15 Horizontal Window Size Right Low Register.

HORIZONTAL WINDOW SIZE LEFT/RIGHT HIGH: Address 0x0D, factory default value 0x00. This register shares horizontal window left high and horizontal window right high.

Horizontal Window Size L/R High								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Value**
0	0	0	0	0	0	0	0	min
0	0	:	:	0	0	:	:	:
0	0	1	1	0	0	1	1	max

Table 3.77. IPX-4M15 Horizontal Window Size Left/Right High Register.

3.9.2 IPX-4M15 Video (AFE) Registers

AFE OPERATION LOW: Address (0x10 ch1; 0x20 ch2), factory default value 0x48.

Operation Low							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	1	0	0	1	0	0	0

Table 3.78a. IPX-4M15 AFE Operation Low Register.

AFE OPERATION HIGH: Address (0x 11 ch1; 0x21 ch2), factory default value 0x00.

Operation High							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	0	0	0	0	0	0	0

Table 3.78b. IPX-4M15 AFE Operation High Register.

AFE CONTROL LOW: Address (0x12 ch1; 0x22 ch2), factory default value 0x04.

AFE Control Low							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	0	0	0	0	1	0	0

Table 3.79a. IPX-4M15 AFE Control Low Register.

AFE CONTROL HIGH: Address (0x13 ch1; 0x23 ch2), factory default value 0x00.

AFE Control High							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	0	0	0	0	0	0	0

Table 3.79b. IPX-4M15 AFE Control High Register.

AFE CLAMP LOW: Address (0x14 ch1; 0x24 ch2), factory default value 0x00.

AFE Clamp Low								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Value**
0	0	0	0	0	0	0	0	min
:	**:**	**:**	**:**	**:**	**:**	**:**	**:**	**:**
1	1	1	1	1	1	1	1	max

Table 3.80a. IPX-4M15 AFE Clamp Low Register.

AFE CLAMP HIGH: Address (0x15 ch1; 0x25 ch2), factory default value 0x00.

AFE Clamp High								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Value**
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0

Table 3.80b. IPX-4M15 AFE Clamp High Register.

AFE GAIN LOW: Address (0x16 ch1; 0x26 ch2), factory default value 0xAA.

AFE Gain Low								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Value**
0	0	0	0	0	0	0	0	min
:	**:**	**:**	**:**	**:**	**:**	**:**	**:**	**:**
1	1	1	1	1	1	1	1	max

Table 3.81a. IPX-4M15 AFE Gain Low Register.

AFE GAIN HIGH: Address (0x17 ch1; 0x27 ch2), factory default value 0x00.

AFE Gain High								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Value**
0	0	0	0	0	0	0	0	min
0	0	0	0	0	0	**:**	**:**	**:**
0	0	0	0	0	0	1	1	max

Table 3.81b. IPX-4M15 AFE Gain High Register.

3.9.3 IPX-4M15 Manufacturing Data Registers

MANUFACTURING DATA: Address (0xB0 to BF)

Address	Contents	Type	Range
B0	Assembly Part Number and Revision Number	HEX	0x00 : 0xFF
B1		HEX	0x00 : 0xFF
B2		HEX	0x00 : 0xFF
B3		HEX	0x00 : 0xFF
B4		ASCII	A : Z, 0: 9
B5		ASCII	A : Z, 0: 9
B6		ASCII	A : Z, 0: 9
B7	Assembly Serial Number	HEX	0x00 : 0xFF
B8		HEX	0x00 : 0xFF
B9		HEX	0x00 : 0xFF
BA	CCD Serial Number	HEX	0x00 : 0xFF
BB		HEX	0x00 : 0xFF
BC		HEX	0x00 : 0xFF
BD	Date of Mfg.	HEX	0x00 : 0xFF
BE		HEX	0x00 : 0xFF
BF		HEX	0x00 : 0xFF

Table 3.82. IPX-4M15 Manufacturing Data Registers

3.10 IPX-11M5 REGISTERS

3.10.1 IPX-11M5 Control Registers

BOOT CONTROL: Address FF, factory default value 0x00.

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	Boot Mode

0 – Boot from Factory settings
1 – Boot from User settings

Table 3.83. IPX-11M5 Boot Control Register.

CAMERA CONTROL 1: Address 0x00, factory default value 0x02.

D7	D6	D5	D4	D3	D2	D1	D0
Horizontal Window enable	Long Integration enable	Shutter enable	Vertical Window enable	Vertical Binning enable	Mirror Image enable	Dual Out enable	Strobe enable

0 - disable
1 - enable

Table 3.84. IPX-11M5 Camera Control 1 Register.

CAMERA CONTROL 2: Address 0x01, factory default value 0x00.

D7	D6	D5	D4	D3	D2	D1	D0
8/10/12 bits 0	Test Mode 1	Test Mode 0	Gamma enable	8/10/12 bits 1	Horizontal Binning enable	CC1 Trigger enable	External Trigger enable

00 – 8 bit
01 – 10 bit
10 – 12 bit

00 - disable
01 - fixed image #1
10 - fixed image #2
11 - moving image

0 - disable
1 - enable

Table 3.85. IPX-11M5 Camera Control 2 Register.

EXTERNAL TRIGGER DURATION: Address 0x02, factory default value 0x01.

External Trigger Duration								
D7	**D6**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**Value**
0	0	0	0	0	0	0	0	min
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	max

Table 3.86. IPX-11M5 External Trigger Duration Register.

VERTICAL WINDOW TOP LINES LOW: Address 0x04, factory default value 0x01.

Vertical Window Top Lines Low								
D7	**D6**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**Value**
0	0	0	0	0	0	0	0	min
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	max

Table 3.87a. IPX-11M5 Vertical Window Top Lines Low Register.

VERTICAL WINDOW TOP LINES HIGH: Address 0x05, factory default value 0x00.

Vertical Window Top Lines High								
D7	**D6**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**Value**
0	0	0	0	0	0	0	0	min
0	0	0	0	:	:	:	:	:
0	0	0	0	1	1	1	1	max

Table 3.87b. IPX-11M5 Vertical Window Top Lines High Register.

VERTICAL WINDOW BOTTOM LINES LOW: Address 0x06, factory default value 0x00.

Vertical Window Bottom Lines Low								
D7	**D6**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**Value**
0	0	0	0	0	0	0	0	min
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	max

Table 3.88a. IPX-11M5 Vertical Window Bottom Lines Low Register.

VERTICAL WINDOW BOTTOM LINES HIGH: Address 0x07, factory default value 0x08.

Vertical Window Bottom Lines High								
D7	**D6**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**Value**
0	0	0	0	0	0	0	0	min
0	0	0	0	:	:	:	:	:
0	0	0	0	1	1	1	1	max

Table 3.88b. IPX-11M5 Vertical Window Bottom Lines High Register.

SHUTTER TIME SELECT LOW: Address 0x08, factory default value 0x01.

Shutter Time Select Low								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Value**
0	0	0	0	0	0	0	0	min
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	max

Table 3.9a. IPX-11M5 Shutter Time Select Low Register.

SHUTTER TIME SELECT HIGH: Address 0x09, factory default value 0x00.

Shutter Time Select High								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Value**
0	0	0	0	0	0	0	0	min
0	0	0	0	:	:	:	:	:
0	0	0	0	1	1	1	1	max

Table 3.89b. IPX-11M5 Shutter Time Select High Register.

LONG INTEGRATION TIME LOW: Address 0x0A, factory default value 0x01.

Long Integration Time Low								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Value**
0	0	0	0	0	0	0	0	min
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	max

Table 3.90a. IPX-11M5 Long Integration Time Low Register.

PRE-EXPOSURE/LONG INTEGRATION TIME HIGH: Address 0x0B, factory default value 0x00. This register shares pre-exposure and long integration high.

Pre-Exposure						Long Integration Time High		
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Value**
PE D5	PE D4	PE D3	PE D2	PE D1	PE D0	LIT D9	LIT D8	
0	0	0	0	0	0	0	0	min
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	max

Table 3.90b. IPX-11M5 Pre-Exposure/Long Integration Time High Register.

STROBE POSITION SELECT LOW: Address 0x0C, factory default value 0x01.

Strobe Position Select Low								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Value**
0	0	0	0	0	0	0	0	min
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	max

Table 3.91a. IPX-11M5 Strobe Position Select Low Register.

STROBE POSITION SELECT HIGH: Address 0x03, factory default value 0x00.

Strobe Position Select High								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Value**
0	0	0	0	0	0	0	0	min
0	0	0	0	:	:	:	:	:
0	0	0	0	1	1	1	1	max

Table 3.91b. IPX-11M5 Strobe Position Select High Register.

HORIZONTAL WINDOW SIZE LEFT LOW: Address 0x0E, factory default value 0x01.

Horizontal Window Size Left Low								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Value**
0	0	0	0	0	0	0	0	min
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	max

Table 3.92a. IPX-11M5 Horizontal Window Size Left Low Register.

HORIZONTAL WINDOW SIZE RIGHT LOW: Address 0x0F, factory default value 0x01.

Horizontal Window Size Right Low								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Value**
0	0	0	0	0	0	0	0	min
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	max

Table 3.92b. IPX-11M5 Horizontal Window Size Right Low Register.

HORIZONTAL WINDOW SIZE LEFT/RIGHT HIGH: Address 0x0D, factory default value 0x00. This register shares horizontal window left high and horizontal window right high.

Horizontal Window Size L/R High								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Value**
0	0	0	0	0	0	0	0	min
0	0	:	:	0	0	:	:	:
0	0	1	1	0	0	1	1	max

Table 3.93. IPX-11M5 Horizontal Window Size Left/Right High Register.

3.10.2 IPX-11M5 Video (AFE) Registers

AFE OPERATION LOW: Address (0x10 ch1; 0x20 ch2), factory default value 0x48.

Operation Low							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	1	0	0	1	0	0	0

Table 3.94a. IPX-11M5 AFE Operation Low Register.

AFE OPERATION HIGH: Address (0x 11 ch1; 0x21 ch2), factory default value 0x00.

Operation High							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	0	0	0	0	0	0	0

Table 3.94b. IPX-11M5 AFE Operation High Register.

AFE CONTROL LOW: Address (0x12 ch1; 0x22 ch2), factory default value 0x04.

AFE Control Low							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	0	0	0	0	1	0	0

Table 3.95a. IPX-11M5 AFE Control Low Register.

AFE CONTROL HIGH: Address (0x13 ch1; 0x23 ch2), factory default value 0x00.

AFE Control High							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	0	0	0	0	0	0	0

Table 3.95b. IPX-11M5 AFE Control High Register.

AFE CLAMP LOW: Address (0x14 ch1; 0x24 ch2), factory default value 0x00.

AFE Clamp Low								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Value**
0	0	0	0	0	0	0	0	min
:	**:**	**:**	**:**	**:**	**:**	**:**	**:**	**:**
1	1	1	1	1	1	1	1	max

Table 3.96a. IPX-11M5 AFE Clamp Low Register.

AFE CLAMP HIGH: Address (0x15 ch1; 0x25 ch2), factory default value 0x00.

AFE Clamp High								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Value**
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0

Table 3.96b. IPX-11M5 AFE Clamp High Register.

AFE GAIN LOW: Address (0x16 ch1; 0x26 ch2), factory default value 0xAA.

AFE Gain Low								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Value**
0	0	0	0	0	0	0	0	min
:	**:**	**:**	**:**	**:**	**:**	**:**	**:**	**:**
1	1	1	1	1	1	1	1	max

Table 3.97a. IPX-11M5 AFE Gain Low Register.

AFE GAIN HIGH: Address (0x17 ch1; 0x27 ch2), factory default value 0x00.

AFE Gain High								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Value**
0	0	0	0	0	0	0	0	min
0	0	0	0	0	0	**:**	**:**	**:**
0	0	0	0	0	0	1	1	max

Table 3.97b. IPX-11M5 AFE Gain High Register.

3.10.3 IPX-11M5 Manufacturing Data Registers

MANUFACTURING DATA: Address (0xB0 to BF)

Address	Contents	Type	Range
B0	Assembly Part Number and Revision Number	HEX	0x00 : 0xFF
B1		HEX	0x00 : 0xFF
B2		HEX	0x00 : 0xFF
B3		HEX	0x00 : 0xFF
B4		ASCII	A : Z, 0: 9
B5		ASCII	A : Z, 0: 9
B6		ASCII	A : Z, 0: 9
B7	Assembly Serial Number	HEX	0x00 : 0xFF
B8		HEX	0x00 : 0xFF
B9		HEX	0x00 : 0xFF
BA	CCD Serial Number	HEX	0x00 : 0xFF
BB		HEX	0x00 : 0xFF
BC		HEX	0x00 : 0xFF
BD	Date of Mfg.	HEX	0x00 : 0xFF
BE		HEX	0x00 : 0xFF
BF		HEX	0x00 : 0xFF

Table 3.98. IPX-11M5 Manufacturing Data Registers

3.11 CAMERA CONFIGURATION UTILITY SOFTWARE

Camera configuration utility software is provided with each camera. After installing the program, the user can program the camera, change it's settings, and save them as a file or in the camera – refer to the application help file. The configuration utility includes an interactive help file, which will guide you through the camera settings and operation features.

3.11.1 Discovery Procedure

Often times multiple frame grabbers and cameras may be installed into a computer at the same time. The CamConfig utility provides an intelligent, automated method of 'discovering' these components and allowing the user to select the one that he is interested in using. When the CamConfig utility is run, it will search the system32 folder for all files which match the clser***.dll naming convention (per the Camera link specification). For each file that it finds, it will open the .DLL and determine how many ports the .DLL supports. It will then communicate with each port and attempt to query the attached camera (if any). If it finds an attached Imperx camera, it will read the 'camera type' information from the camera. It will then display a list box, which includes all DLLs, ports and cameras that it discovered. The user can then select the DLL/port/camera, that he is interested in using, by highlighting the entry and clicking on the 'OK' button. Clicking on the 'Rescan Ports' button causes the above discovery procedure to be repeated.

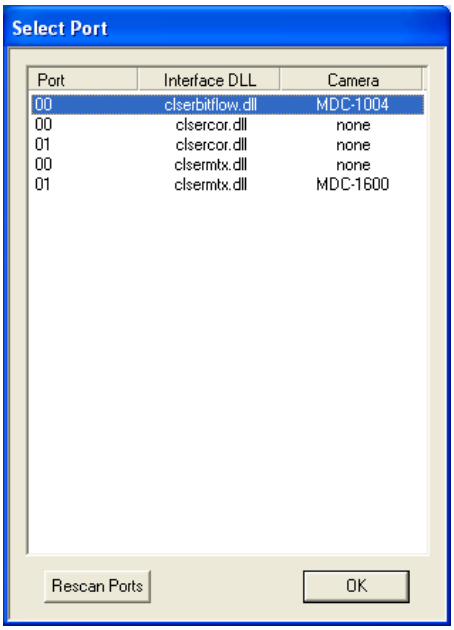


Figure 42. Select Port dialog

3.11.2 Usage

After having selected the desired camera, the main Camera Configuration utility dialog will appear. The graphical user interface is very intuitive and self-explanatory. The configuration utility includes an interactive help file, which will guide you through the GUI controls and camera settings.

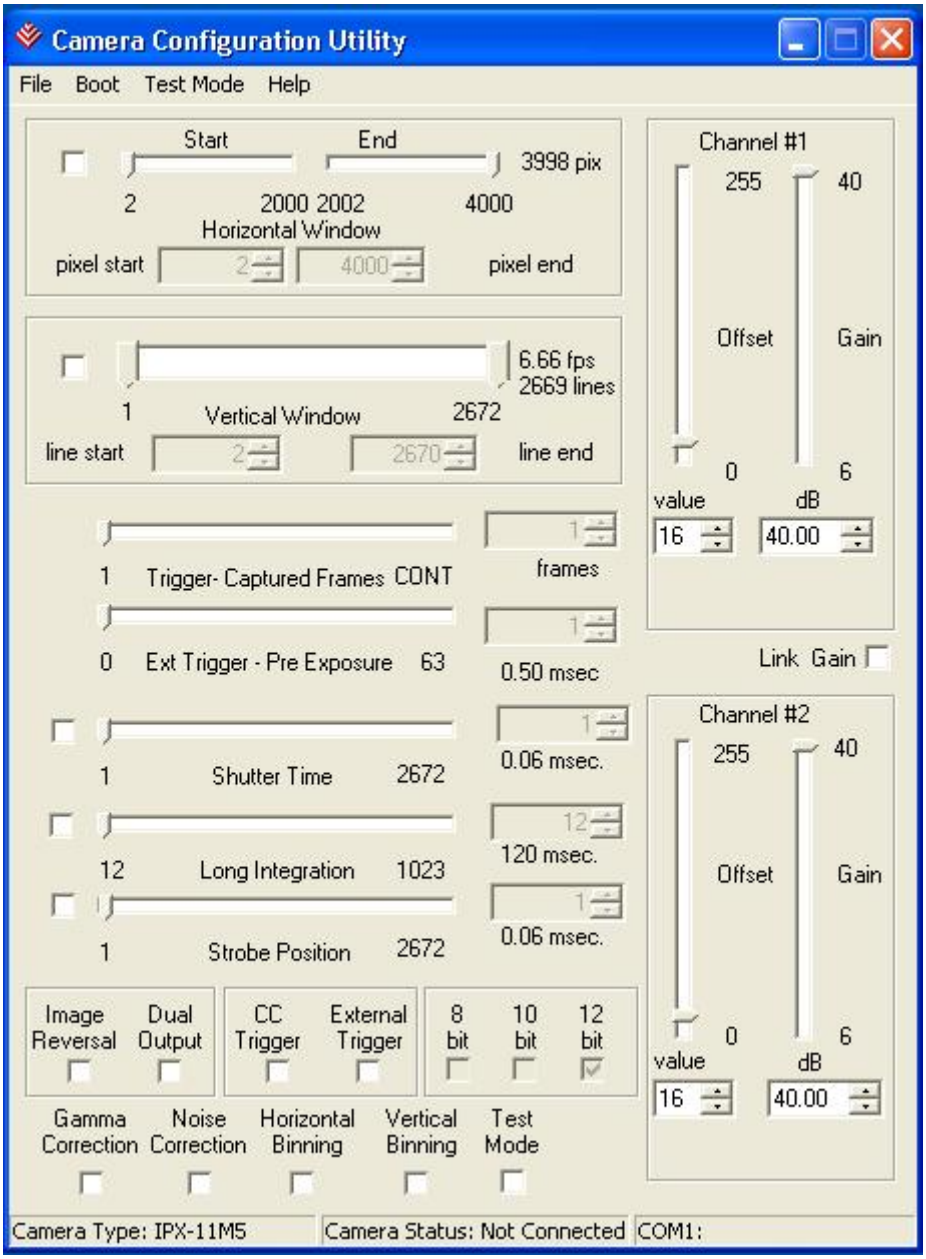


Figure 43. IPX Configurator graphical user interface

IPX Warranty and Support

This chapter discusses the camera's warranty and support.

4.1 ORDERING INFORMATION

Ordering: **IPX-11M5 - C F**

Camera Model

VGA120
VGA210
1M48
2M30
2M30H
4M15
11M5

Lens Mount

C - "C" mount
F - "F" mount
O - Open frame

Sensor Type

M - Monochrome
C - Color
U - UV sensitive (no glass)
S - Special - user filter

For any other custom camera configurations, please contact Imperx, Inc.

4.2 TECHNICAL SUPPORT

Each camera is fully tested before shipping. If for some reason the camera is not operational after power up please check the following:

1. Check the power supply and all I/O cables. Make sure that all the connectors are firmly attached.
2. Check the status LED and verify that is steady ON, if not – refer to the LED section.
3. Enable the test mode and verify that the communication between the frame grabber and the camera is established. If the test pattern is not present, power off the camera, check all the cabling, frame grabber settings and computer status.
4. If you still have problems with the camera operation, please contact technical support:

Email: techsupport@imperx.com
Toll Free (866) 849-1662 or (+1) 561-989-0006
Fax: (+1) 561-989-0045
Visit our Web Site: www.imperx.com

4.3 WARRANTY

Imperx warrants performance of its products and related software to the specifications applicable at the time of sale in accordance with Imperx' s standard warranty, which is 1 (one) year parts and labor. **For glassless cameras the CCD is NOT covered by the warranty.**

Do not open the housing of the camera. Warranty voids if the housing has been open or tampered.

IMPORTANT NOTICE

This camera has been tested and complies with the limits of Class A digital device, pursuant to part 15 of the FCC rules.

Imperx reserves the right to make changes to its products or to discontinue any product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

IMPERX PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Software Installation

This appendix explains how to install the IPX software.

A.1 Software Suite

The IPX software suite consists of the following files:

Windows XP and 2000 application files:
(located in c:\Program_Files\ImperX\IPX\ )

IPX_Configurator.exe	- IPX Configurator application
IPX_config.ini	- Configuration settings
IPX_config.chm	- Compiled HTML help file
mfc70u.dll	- Windows DLL
msvcp70.dll	- Windows DLL
msvcr70u.dll	- Windows DLL

Documentation files:
(located in c:\Program_Files\ImperX\IPX\Doc\ )

IPX_Users_Manual.pdf

A.2 Software Installation from CD

Use the following steps to install the IPX software supplied on a CD:

1. If a version of IPX was previously installed on this machine, then you must first remove it:

   1.1 Left mouse click on *"Start"*
   1.2 Left mouse click on *"Settings"*.
   1.3 Left mouse click on *"Control Panel"*.
   1.4 Double left mouse click on *"Add or Remove Programs"*.
   1.5 Left mouse click *"IPX Software"*.
   1.6 Left mouse click on *"Remove"*.
   1.7 Left mouse click on *"Yes"*.
   1.8 Left mouse click on *"Close"*.
   1.9 If the 'IPX Software - InstallShield Wizard' pops-up:
   - Left mouse click on 'Remove'.
   - Click 'Next'.
   - Click 'Yes'.
   - Click 'Finish'.

2. Software Installation from CD

2.1 Insert the IPX CD into the appropriate drive; the setup.exe file will run automatically. Note: If it does not start automatically, left mouse click on to *"Start"*, *"Run"*, enter or browse to*"(CD drive): setup.exe"* and click *"OK"*.
2.2 Wait for the "IPX Software - InstallShield Wizard" screen to appear.
2.3 Follow the on-screen instructions.
2.4 When finished a new "IPX Configurator" icon will appear on the desktop.

A.3 Software Upgrade from Web Site

New application and/or driver software may be released periodically to reflect improvements and/or functionality added to the IPX camera. You can retrieve these updates by visiting the download page of our web site at http://www.imperx.com/downloads.asp.

1. Use the following steps to install newly released application software:

1.1 Uninstall all application and driver files by following the instructions in step 1. of the 'Software Installation from CD' section.
1.2 Download the IPX_Installer_x_x_x_x.exe file (x represents the revision) from the Imperx web site to a new folder on your PC (we will use the folder C:\new_IPX as an example).
1.3 Left mouse click on *"Start"*, *"Run"* then enter or browse to *"C:\new_IPX\ IPX_Installer_x_x_x_x.exe"*.
1.4 Wait for the "IPX Software - InstallShield Wizard" screen to appear.
1.5 Follow the on-screen instructions.
1.6 When finished a new "IPX Configurator" icon will appear on the desktop.